ENHANCEMENT OF POWER QUALITY USING MULTILEVEL INVERTERS BY ACTIVE FAULT TOLERANT CONTROL SYSTEM

P.Prabhakar,
Assistant Professor,
Department Of EEE
Christu Jyothi Institute Of Technology &Science, Colombo Nagar, Telangana.

Y.Vijay Jawahar Paul,
Assistant Professor,
Department Of EEE
Christu Jyothi Institute Of Technology &Science,Colombo Nagar,Telangana.

SD.Farzana,
Assistant Professor,
Department Of EEE
Christu Jyothi Institute Of Technology & Science, Colombo Nagar, Telangana.

G.Jyothi
Student
Department Of EEE
Christu Jyothi Institute Of Technology & Science, Colombo Nagar, Telangana.

ABSTRACT

The integration of renewable energy sources and the increasing complexity of power systems demand advanced control strategies for inverters to ensure reliable and high-quality power supply. This research focuses on the design of an active fault-tolerant control system for multilevel inverters, aiming to enhance systems power quality. The proposed system combines fault detection, isolation, and compensation mechanisms to mitigate the impact of faults and disturbances, providing a robust and resilient solution for modern power system. Multilevel inverters have gained prominence in power electronics due to their ability to generate high-quality output voltage with reduced harmonic distortion. The growing emphasis on renewable energy integration and the increasing complexity of power grids necessitate the development of fault-tolerant control systems for multilevel inverters. This research aims to address this need by proposing an active fault-tolerant control strategy.

INTRODUCTION

Multilevel converters have been mainly used in medium- or high-power system applications, such as static reactive power compensation and adjustable-speed drives. In these applications, due to the limitations of the currently available power semiconductor technology, a multilevel concept is usually a unique alternative because it is based on low-frequency switching and provides voltage and/or current sharing between the power semiconductor. Fault of switching device can be classified as an openfault and a short-fault The open-circuit switch fault, usually called the open-fault, can occur due to the several reasons such as a damaged inner wire, a momentary short circuit and, gate driver fault. The short-fault can occur due to the several reasons such as overvoltage, overcurrent, breakdown of the protection components and wrong gate signal. The short-fault is difficult to handle because an abnormal overcurrent which can cause serious damage to other parts is produced immediately. Regarding the open circuit faults in a 9-level cascaded MLI, it is clear that there are 16 switches for each phase. From this one can infer that the total no. of switches for a 3-φ 9-level Cascaded MLI will be 48 which is quite a tedious task to determine the faulty switch location for which an algorithm was developed to find out if the faulty switch has an open circuit fault.

An FTC's primary function is to avoid malfunctions in important systems that might lead to their failure. One of the strategies used to construct an FTC system is redundancy, which is divided into two categories: anaytical redundancy and hardware redundancy. Active and passive analytical redundancy are the two types of redundancy.

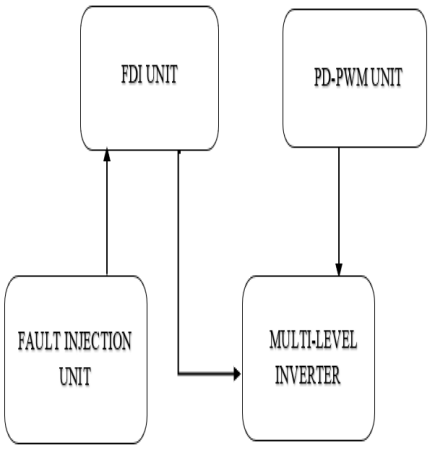


Fig 1. Proposed configuration

The Fault Detection and Isolation (FDI) unit is the most important part of an Active Fault-Tolerant Control System (AFTCS), and it is responsible for detecting problems. The FDI performs controller reconfiguration after recognizing and isolating a malfunction by employing the estimated parameter values by the observer to adopt new circumstances. The Phase Disposition Pulse Width Modulation (PD-PWM) technique has been utilized for switching due to its superior performance as compared to other conventional techniques. This early fault detection method not only identified the issues but also performed preventative actions to keep the system healthy and stable. The proposed system was experimentally tested on the MATLAB / Simulink environment to verify its performance

LITERATURE REVIEW

Multilevel Inverter Topologies for Standalone PV Systems (S. Daher, J. Schmid, F. L. M. Antunes, IEEE Trans. Ind. Electron., Jul. 2008). Daher et al. presented innovative multilevel inverter topologies specifically tailored for stand-alone Photovoltaic (PV) systems [1]. The paper delves into advanced techniques for enhancing the efficiency and reliability of PV systems through the integration of multilevel inverters, catering to the unique requirements of standalone applications. Modulation and Voltage Balancing of a Five-Level Series-Connected Multilevel Inverter with Reduced Isolated Direct Current Sources (Dekka, O. Beik, M. Narimani, IEEE Trans. Ind. Electron., Oct. 2020). Dekka et al. proposed a modulation and voltage balancing strategy for a fivelevel series-connected multilevel inverter [2]. Emphasizing the reduction of isolated direct current sources, the study addresses key challenges in achieving optimal performance and balance in multilevel inverter configurations. Five-level Cascade Asymmetric Multilevel Converter (S. A. González, M. I. Valla, C. F. Christiansen, IET Power Electron., 2010). The authors presented a comprehensive exploration of a five-level cascade asymmetric multilevel converter, contributing insights into its design and operational characteristics [3]. This work contributes to the understanding of unique topologies within the multilevel inverter domain. Single-stage Switchedcapacitor Module (S3CM) Topology for Cascaded Multilevel Inverter (S. S. Lee, IEEE Trans. Power Electron., Oct. 2018) Lee introduced the Single-stage Switchedcapacitor Module (S3CM) topology, a noteworthy innovation for cascaded multilevel inverters [4]. This novel approach addresses challenges in achieving optimal performance in multilevel inverter configurations, particularly focusing on the simplification of the circuit topology. The Seven-level Flying Capacitor Based ANPC Converter for Grid Integration of Utilityscale PV Systems (G. Konstantinou, S. R. Pulikanti, M. Ciobotaru, V. G. Agelidis, K. Muttaqi, Proc. 3rd IEEE Int. Symp. Power Electron. Distrib. Gener. Syst. (PEDG), Jun. 2012) Konstantinou et al. presented a sevenlevel flying capacitor-based Active Neutral Point Clamped (ANPC) converter designed for grid integration in utility-scale PV systems [5]. This contribution explores the potential of multilevel inverters in largescale renewable energy applications. A Novel Way to Deal with Harmonic Elimination in Multi-Level

CHB Inverter Using Without Filtering Technique (P. N. V. S. Ayyappa, C. Srinivas, T. R. S. Singh, Proc. Int. Conf. Electron., Commun. Aerosp. Technol. (ICECA), Apr. 2017). Ayyappa et al. proposed an innovative approach to harmonic elimination in multilevel CHB inverters without relying on filtering techniques [6]. This study addresses challenges in achieving harmonicfree operation in multilevel inverters, contributing to the broader field of power quality enhancement. Active Fault-Tolerant Control Design for Nonlinear Systems (R. Abbaspour, M.S. thesis, FIU Electron., 2018). Abbaspour's thesis focuses on the design of active fault-tolerant control systems for nonlinear systems [7]. The study explores strategies to enhance the reliability and fault tolerance of multilevel inverter systems, contributing valuable insights to the broader domain of faulttolerant control. Fault-tolerant Control of Cascaded H-bridge Converters Using Double Zero-sequence Voltage Injection and DC Voltage Optimization (Z. Ji, J. Zhao, Y. Sun, X. Yao, Z. Zhu, J. Power Electron., Sep. 2014). Ji et al. presented a fault-tolerant control strategy for cascaded H-bridge converters, incorporating double zero-sequence voltage injection and DC voltage optimization [8]. The study focuses on improving the reliability and robustness of multilevel inverters in the presence of faults. A Review of Fault Tolerant Control Systems: Advancements and Applications (A. Amin, K. M. Hasan, Meas., J. Int. Meas. Confederation, Sep. 2019). Amin and Hasan conducted a comprehensive review of advancements and applications in faulttolerant control systems [9]. The review provides a broad overview of strategies to enhance the fault tolerance of multilevel inverter systems, highlighting key advancements in the field. Intelligent Failure-tolerant Control (R. F. Stengel, IEEE Control Syst. Mag., Jun. 1991). Stengel's work delves into the concept of intelligent failure-tolerant control systems, providing foundational insights into intelligent control strategies for addressing failures in complex systems [10]. While not directly focused on multilevel inverters, the principles discussed have implications for fault-tolerant control in diverse applications.

FAULT ANALYSIS

An n-level CHB MLI requires (n-1)×2 power semiconductor switching devices and (n-1)/2 separate DC sources. The cell output voltage for the first cell can be given as follows:

$$V_{CX1} = (S_1 - S_2) \times E_{DC}$$

where, V_{CX1} = first cell output voltage for X^{th} phase; S_1, S_2 = switching functions (0 or 1) for S_{X1}, S_{X2}; and E_{DC} = DC voltage source.

Similarly, total phase output voltage can be calculated for M cells connected in series

$$E_{OX} = V_{CX1} + V_{CX2} + V_{CX3} + - - - + V_{CXM}$$

The fault-detection algorithm is presented in Figure in this section. The process of faulty switch identification occurs in two parts: (i) THD measurement and (ii) normalized voltage factor. The first of these can identify the faulty switch phase. The THD value of the faulty switch phase will be comparatively higher than that of the other two phases. Normalization of the output phase voltage is taken in the second part. Based on the normalized factor value with the threshold comparison, the probable switch fault location can be identified.

(i) Total harmonic distortion measurement of output phase voltage

The THD is measured from the output phase voltage using fast Fourier transform (FFT). It can be calculated as follow

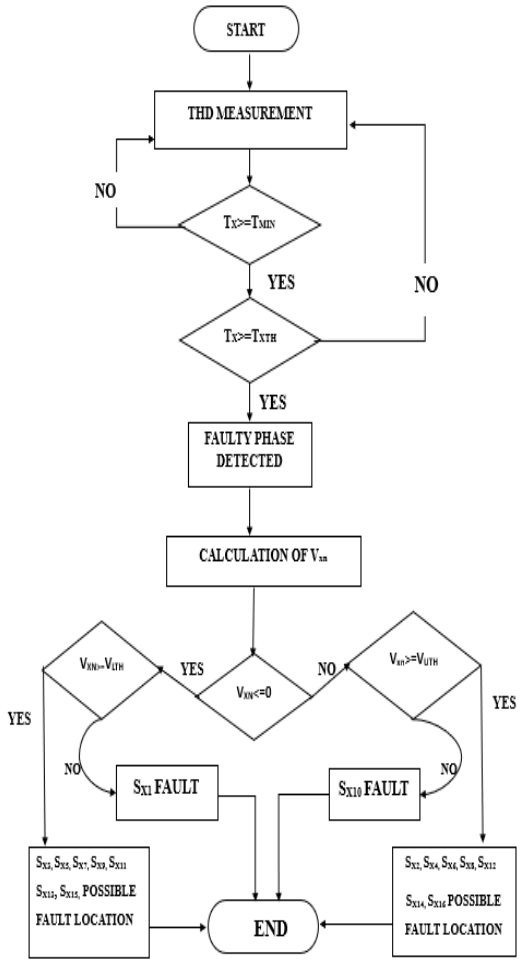
$$THD(T_X) = \frac{\sqrt{\sum_{h=2}^{hmax} E_{OXh}^2}}{E_{OX1}} \times 100$$

If the OCSF occurs in any X^{th} phase switch, the THD (T_X) of that particular phase will be comparatively higher than it is for the other two phases. The value of T_X is compared with the minimum THD threshold named T_{MIN}. The measured value of T_X is compared with the switch fault THD threshold, called T_{Xth}. It is the threshold-defined value of the THD count for OSCF conditions. Once the faulty phase is identified, the normalized factor for the output phase voltage will be calculated.

(ii) Normalized voltage factor:
The normalized voltage factor (V_{Xn}) of each phase can be given as the ratio of the average voltage (V_{Xav}) of the respective phase and the Park's transformation of the output voltage (V_S).

$$VX_n = \frac{VX_{AV}}{V_S}$$

$$V_S = V_d + V_q$$



PROPOSED SYSTEM CONFIGURATION

The proposed fault-tolerant control system for IGBT-based 9-level cascaded MLI has been implemented in MATLAB and Simulink environment To explain this model in a better way, it has been divided into four major parts i.e. phase disposition-based pulse width modulation system, fault detection, and isolation system, and power electronics-based model of 9 levels cascaded MLI.

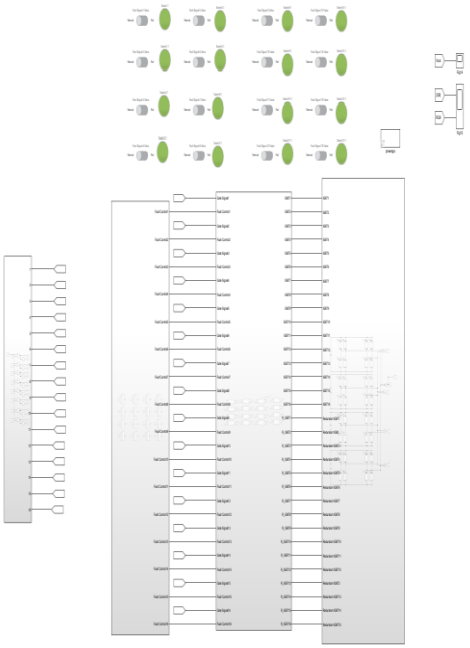


Fig 2. Proposed FT-CHB-MLI model

The model consists of individual subunits as follows:

1. Fault Injection Unit
2. Phase Disposition Unit
3. Fault Injection Block
4. Fault Detection and Isolation Unit
5. 9-Level CHB MLI

The Fault Injection Unit (FIU) in which the control of 16 IGBT switches has been used. The switch is made by pressing the slider switch to the Fail position. The fault control block receives the command from the FIU. For the true value of the switch, the value of 1 is passed and for a faulty switch, the ramp down signal is passed with becomes zero after a time delay of 0.2 sec. The proposed redundant, fault-tolerant system is implemented for the operation of 9-levels cascaded MLI in Simulink

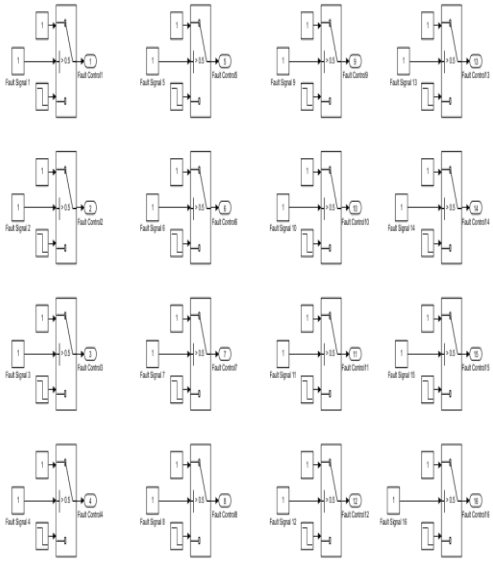


Fig 3. Fault injection unit

The FDI unit, is one of the main components of the project and is an essential component of an AFTCS architecture. It consists of the control system for two different outputs i.e. one from the main IGBT and the other from the standby IGBT. During normal operation, output from the regular IGBT is provided to the power circuit. However, in case of fault, the faulty switch is located and isolated. The output from the standby switch is then provided to the power circuit with a slight delay incorporated as per the practical scenario. The internal blocks for the switches in the FDi. The fault detection unit of the FDI unit has two indications. The first is a constant zero signal block, which indicates that the redundant IGBT is turned off while the primary IGBT. FT-CHB-MLI simulink switches model. is operational. The second signal, is the healthy signal, which is utilized to turn on the primary IGBT. The fault control signal actuates the switch and isolates the faulty switch by supplying no gate signal to it while simultaneously applying the gate signal to redundant IGBTs as the fault is injected. The work assumes that the switching activity of IGBTs takes place in zero time a redundant standby . FTC switching model.

switch. Total harmonic distortion and the determination of a normalized output voltage factor are employed for fault diagnosis.

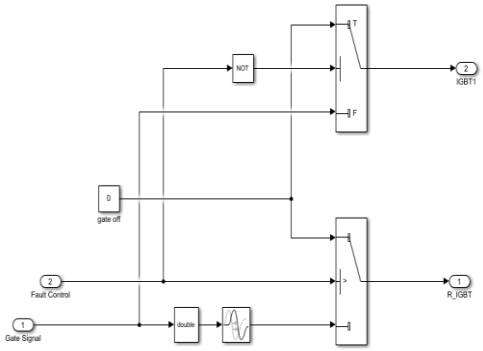


Fig 4. Switching control of the FDI unit

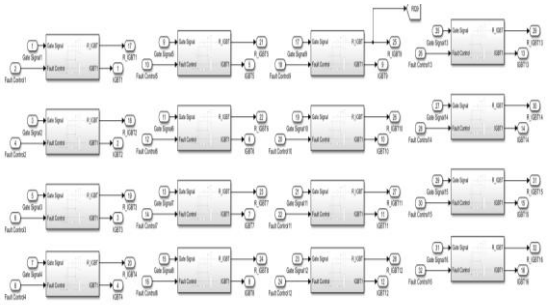


Fig 5. FDI INTERNAL UNIT

The Phase Disposition Pulse Width Modulation (PD-PWM) technique was utilized for switching due to its superior performance as compared to other conventional techniques. As it can be seen that the reference signal here is taken as sine wave and carrier waves are triangular waves which are 8 in number. Relational operator blocks namely lesser than or equal and greater than or equal to are taken based on the requirement. It compares the magnitude of reference signal with carrier signal. Whenever the magnitude of the carrier signal is greater than the reference signal pulse is generated and if the magnitude of the carrier signal is lesser than the reference signal pulse is not generated. Symbolising this condition a NOT Gate has been used.

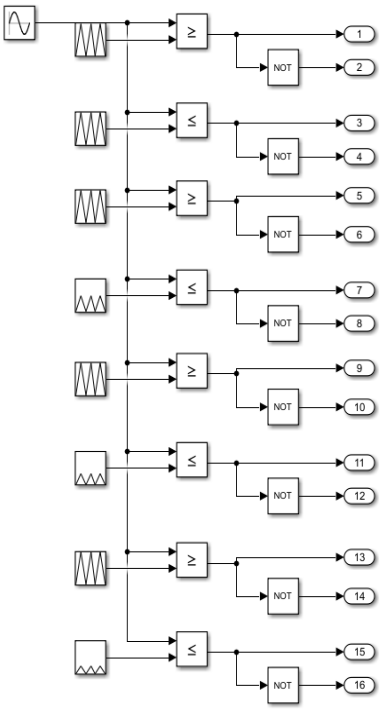


Fig 6. Phase disposition PWM

A 9 level multilevel cascaded H-Bridge inverter has been used so that an approximate sine wave can be generated. No. of DC sources required are m=2(s)+1, where m=no.of levels s=no.of DC sources required. A total of (n - 1) × 2 power devices used for switching devices are needed for an n-level cascaded H-Bridge Multi-Level Inverter. The switching device used here is IGBT. Same no.of redundant switches have been used as that of original ones.

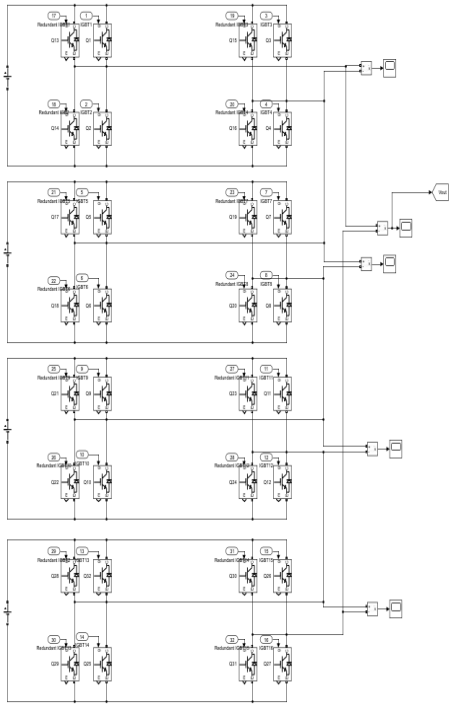


Fig 7. 9-level multi level inverter

RESULTS

The output voltages of the proposed 9-level cascaded MLI has been depicted here. These output voltages have a magnitude of 400V (peak). As in this situation, there is no fault applied at any switch of the MLI, output voltages are equal throughout the simulations.

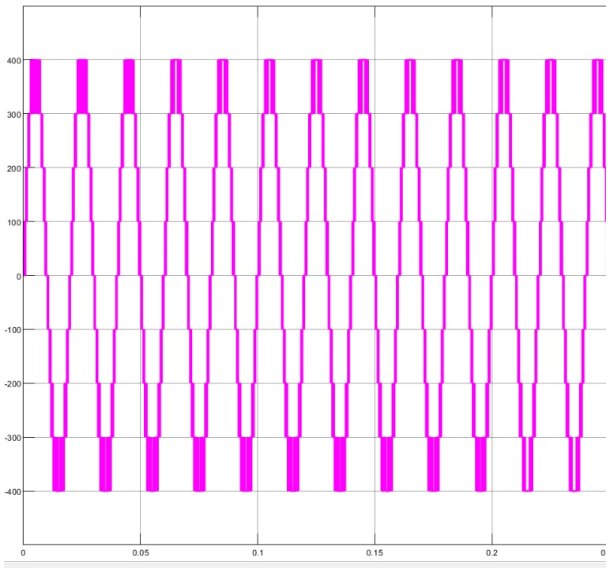


Fig 8. 9-level Voltage waveform without fault

The first part of the waveform represents the IGBT switchs' position under no fault condition, the second part of the figure is representing the Redundant switchs' position when there is no fault. The switching signals to the primary IGBTs during normal operation remains ON. The standby redundant IGBTs remain in the off condition with no switching signal.

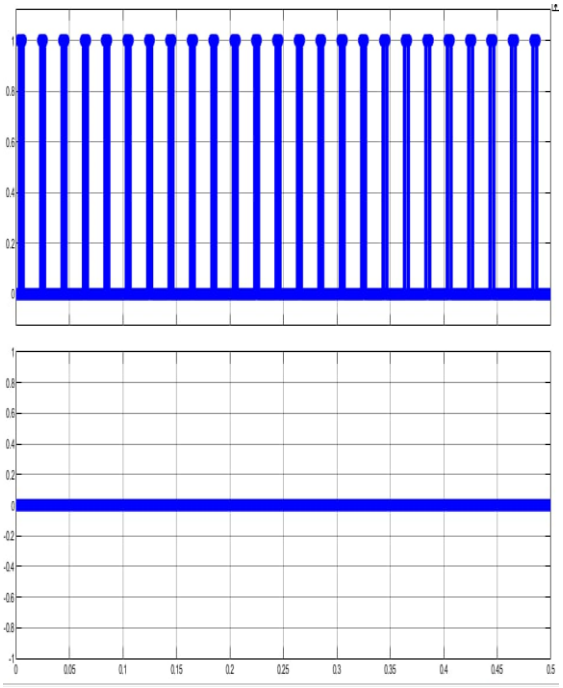


Fig 9. switching pattern without fault

The system has been simulated with FTC CHB MLI configuration and the resulting waveform. The results show that the output is affected at 0.1 seconds at the time of fault injection but returns to its normal operation due to the switch over of the faulty switch to the healthy standby IGBT switch..

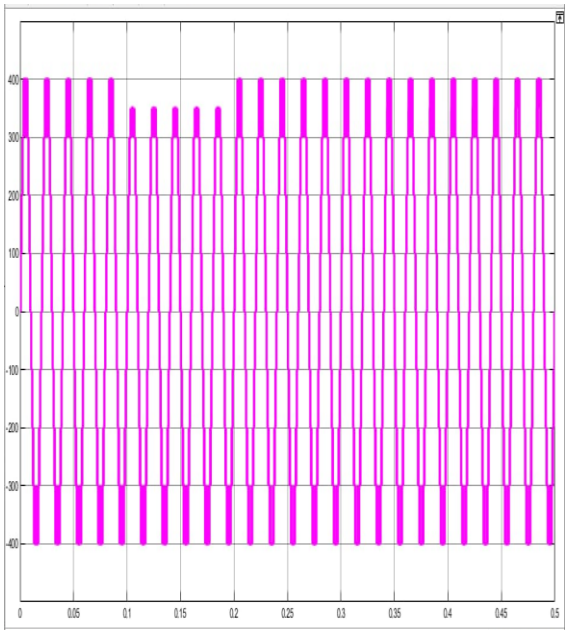


Fig 10. waveform with fault

The switching states of both primary and standby IGBTs after the occurrence of fault is illustrated. It shows the operation of the redundant switch due to the failure of the primary switch.

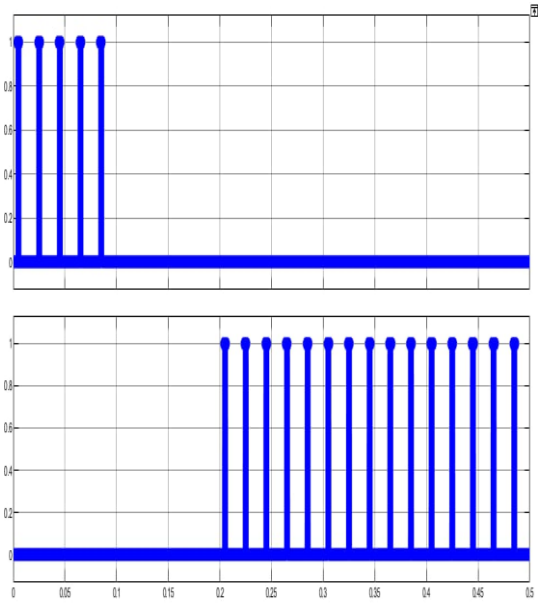


Fig 11. switching pattern with fault

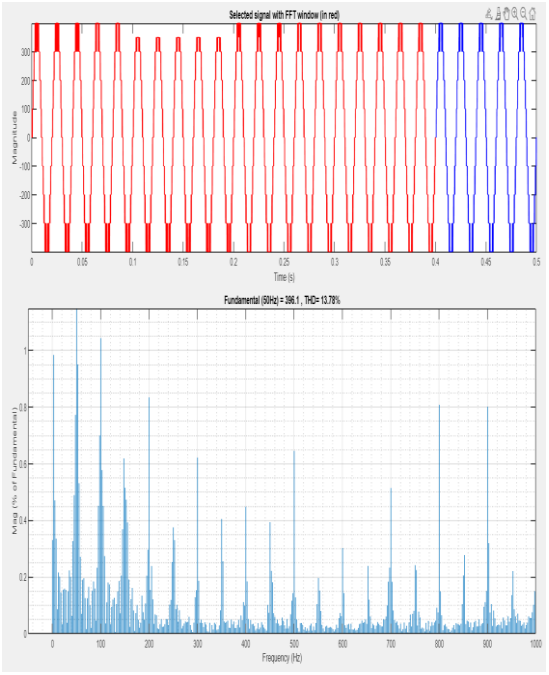


Fig 12. THD with FDI

It can be observed from the figure that, under fault conditions when redundant switches are in working the Total Harmonic Distortion is 13%. Hence, the objective of improving power quality has been successfully achieved.

TABLE 1: COMPARISON WITH REFERENCE

Component	Reference	Proposed Work
THD	18%	13%
No.of switches	12	16
No.of levels	7	9

CONCLUSION

In this project, a novel 9-level Fault-Tolerant Cascaded H-Bridge Multilevel Inverter (FT-CHB-MLI) was proposed TO improved power quality. A dedicated Fault Detection and isolation (FDI) unit was built to diagnose the faulty switch and replace it with a standby redundant switch. Total harmonic distortion and the determination of a normalized output voltage factor were employed for fault

diagnosis. Active FT-CHB-MLIs to achieve Improved Power Quality Width Modulation (PD-PWM) technique was utilized for switching due to its superior performance as compared to other conventional techniques. The proposed system was tested on the MATLAB / Simulink environment to verify its performance. The simulation results demonstrated that the THD has been reduced to almost 13% with a significant increase in reliability with advanced fault-tolerant architecture consisting of FDI units.. A comparison of the proposed work with literature also depicted its superior performance in achieving its superior power quality

FUTURE SCOPE

A more sophisticated FTC technique using artificial intelligence in the future could more precisely pinpoint the Fault location with a better understanding with hardware experimental verification. Another direction is to study the effect of load variations and variations in the modulation index on the performance proposed AFTCS.

REFERENCES

[1] S. Daher, J. Schmid, and F. L. M. Antunes, "Multilevel inverter topologies for stand-alone PV systems," IEEE Trans. Ind. Electron., vol. 55, no. 7, pp. 2703–2712, Jul. 2008, doi: 10.1109/TIE.2008.922601.

[2] A. Dekka, O. Beik, and M. Narimani, "Modulation and voltage balancing of a five-level series-connected multilevel inverter with reduced isolated direct current sources," IEEE Trans. Ind. Electron., vol. 67, no. 10, pp. 8219–8230, Oct. 2020, doi: 10.1109/TIE.2019.2949537.

[3] S. A. González, M. I. Valla, and C. F. Christiansen, "Five-level cascade asymmetric multilevel converter," IET Power Electron., vol. 3, no. 1, p. 120, 2010, doi: 10.1049/iet-pel.2008.0318.

[4] S. S. Lee, "Single-stage switched-capacitor module (S3CM) topology for cascaded multilevel inverter," IEEE Trans. Power Electron., vol. 33, no. 10, pp. 8204–8207, Oct. 2018, doi: 10.1109/TPEL.2018.2805685.

[5] G. Konstantinou, S. R. Pulikanti, M. Ciobotaru, V. G. Agelidis, and K. Muttaqi, "The seven-level flying capacitor based ANPC converter for grid intergration of utility-scale PV systems," in Proc. 3rd IEEE Int. Symp. Power Electron. Distrib. Gener. Syst. (PEDG), Jun. 2012, pp. 592–597.

[6] P. N. V. S. Ayyappa, C. Srinivas, and T. R. S. Singh, "A novel way to deal with harmonic elimination in multi level CHB inverter using without filtering technique," in Proc. Int. Conf. Electron., Commun. Aerosp. Technol. (ICECA), Apr. 2017, pp. 62–67.

[7] A. R. Abbaspour, "Active fault-tolerant control design for nonlinear systems," M.S. thesis, FIU Electron., 2018, vol. 3917. [Online]. Available: https://digitalcommons.fiu.edu/etd/3917

[8] Z. Ji, J. Zhao, Y. Sun, X. Yao, and Z. Zhu, "Fault-tolerant control of cascaded H-bridge converters using double zero-sequence voltage injection and DC voltage optimization," J. Power Electron., vol. 14, no. 5, pp. 946–956, Sep. 2014.

[9] A. A. Amin and K. M. Hasan, "A review of fault tolerant control systems: Advancements and applications," Meas., J. Int. Meas. Confederation, vol. 143, pp. 58–68, Sep. 2019, doi: 10.1016/j.measurement.2019. 04.083.

[10] R. F. Stengel, "Intelligent failure-tolerant control," IEEE Control Syst. Mag., vol. 11, no. 4, pp. 14–23, Jun. 1991.

[11] A. A. Amin and K. Mahmood-Ul-Hasan, "Advanced fault tolerant air-fuel ratio control of internal combustion gas engine for sensor and actuator faults," IEEE Access, vol. 7, pp. 17634–17643, 2019.

[12] M. Sandhu and T. Thakur, "Modified cascaded H-bridge multilevel inverter for hybrid renewable energy applications," IETE J. Res., vol. 1, pp. 1–13, Jul. 2020.

[13] J.-H. Lee and K.-B. Lee, "A fault detection method and a tolerance control in a single-phase cascaded H-bridge multilevel inverter," IFACPapersOnLine, vol. 50, no. 1, pp. 7819–7823, Jul. 2017.

[14] Z. Liu, Y. Lu, J. Kong, J. Gong, and S. Wang, "Multimodal fault-tolerant control for single-phase cascaded off-grid PV-storage system with PV failure using hybrid modulation," Microelectron. Rel., vol. 114, Nov. 2020, Art. no. 113772.

[15] S. Khomfoi and L. M. Tolbert, "Fault detection and reconfiguration technique for cascaded H-bridge 11-level inverter drives operating under faulty condition," in Proc. 7th Int. Conf. Power Electron. Drive Syst., Nov. 2007, pp. 1035–1042.

[16] S. Ahmed, A. A. Amin, Z. Wajid, and F. Ahmad, "Reliable speed control of a permanent magnet DC motor using fault-tolerant H-bridge," Adv. Mech. Eng., vol. 12, no. 10, 2020, Art. no. 1687814020970311.

[17] A. A. Amin and K. Mahmood-ul-Hasan, "Robust active fault-tolerant control for internal combustion gas engine for air–fuel ratio control with statistical regression-based observer model," Meas. Control, vol. 52, nos. 9–10, pp. 1179–1194, Nov. 2019.

[18] K.-H. Chao and C.-H. Ke, "Fault diagnosis and tolerant control of threelevel neutral-point clamped inverters in motor drives," Energies, vol. 13, no. 23, p. 6302, Nov. 2020.

[19] U. Riaz, M. Tayyeb, and A. A. Amin, "A review of sliding mode control with the perspective of utilization in fault tolerant control," Recent Adv. Electr. Electron. Eng., Formerly Recent Patents Electr. Electron. Eng., vol. 14, no. 3, pp. 312–324, Apr. 2021.

[20] P. Lezana, R. Aguilera, and J. Rodríguez, "Fault detection on multicell converter based on output voltage frequency analysis," IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 2275–2283, Jun. 2009.

[21] J. Druant, T. Vyncke, F. De Belie, P. Sergeant, and J. Melkebeek, "Adding inverter fault detection to model-based predictive control for flying-capacitor inverters," IEEE Trans. Ind. Electron., vol. 62, no. 4, pp. 2054–2063, Apr. 2015.

[22] H.-W. Sim, J.-S. Lee, and K.-B. Lee, "Detecting open-switch faults: Using asymmetric zero-voltage switching states," IEEE Ind. Appl. Mag., vol. 22, no. 2, pp. 27–37, Mar. 2016.

[23] A. A. Amin and K. Mahmood-ul-Hasan, "Hybrid fault tolerant control for air–fuel ratio control of internal combustion gasoline engine using Kalman filters with advanced redundancy," Meas. Control, vol. 52, nos. 5–6, pp. 473–492, Jun. 2019, doi: 10.1177/0020294019842593.

[24] R. Sarker, "Phase disposition PWM (PD-PWM) technique to minimize WTHD from a three-phase NPC multilevel voltage source inverter," in Proc. IEEE 1st Int. Conf. Converg. Eng. (ICCE), Sep. 2020, pp. 220–224, doi: 10.1109/ICCE50343.2020.9290697.

[25] D. Ronanki and S. S. Williamson, "Modified phase-disposition PWM technique for modular multilevel converters," in Proc. IEEE Transp. Electrific. Conf. Expo (ITEC), Jun. 2018, pp. 26–31, doi: 10.1109/ITEC.2018.8450084.

[26] Y. Zang, X. Wang, B. Xu, and J. Liu, "Control method for cascaded H-bridge multilevel inverter failures," in Proc. 6th World Congr. Intell. Control Autom., vol. 2, 2006, pp. 8462–8466. [27] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002. [28] M. Abdelsalam, H. Diab, S. Tennakoon, and A. Griffiths, "Reliability enhancement of modular multilevel converter by applying fault tolerant control," in Proc. 51st Int. Univ. Power Eng. Conf. (UPEC), Sep. 2016, pp. 1–5, doi: 10.1109/UPEC.2016.8114008. [29] P. Mehta, S. Sahoo, and M. Kumar, "A fault-diagnosis and tolerant control technique for five-level cascaded H-bridge inverters," IET Circuits, Devices Syst., vol. 15, no. 4, pp. 366–376, 2021.