DESIGN AND ANALYSIS OF FULL ADDER BASED ON DOMINO LOGIC TECHNIQUE

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ABSTRACT: Full adder is one of the basic blocks for many such VLSI circuits to perform multiplication, division and exponentiation operations. The demands of upcoming computing, as well as the challenges of nanometer-era of VLSI design necessitate new digital logic techniques and styles that are at the same time high performance, energy efficient and robust to noise and variation. Dynamic CMOS logic gates are broadly used to design high performance circuits due to their high speed. Circuit design using domino logic tends to be a very attractive method for high speed and low delay designs. Therefore Domino Logic based high performance full adder design is proposed in our project.

KEYWORDS: Very Large Scale Integration (VLSI), Full adder, Domino Logic.

INTRODUCTION: In the fast-growing VLSI industry, transistor density is increasing with rapid rate day-by-day. According to Moore's law transistor density will get doubled itself after every eighteen months. So, a technology is required by which the area can be reduced and increase the performance of the device. So, it requires to switch to a technology, which uses lesser area and smaller delay. Hence, the Domino logic is used for designing the one-bit full adder and compared the various performance parameter like area, delay, and power consumption in both technologies.

Domino logic

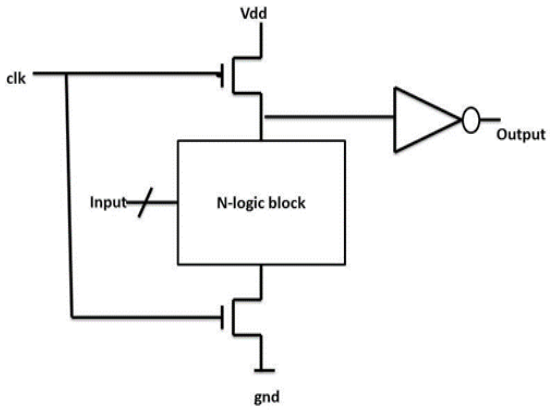

Fig: Domino logic.

A static inverter is used between the two stages for removing the drawback of dynamic logic. There are various advantages of Domino logic like they have a smaller area unlike conventional CMOS logic, parasitic

capacitance are smaller in domino logic so it provide high speed of operation and result is *glitch* free because each gate makes only one transition.

DESIGNING TECHNIQUES: Two design techniques will be used for the analysis of full - adder circuit, namely CMOS based logic style and domino-based logic and provided their comparative results. An adder is a digital circuit that is used for performing the addition of numbers. In calculator and computers, adders are used in arithmetic and logic units. This combinational circuit takes three inputs which are one-bit each, named as A, B and C. It consists hastwo outputs named as the sum and carry.

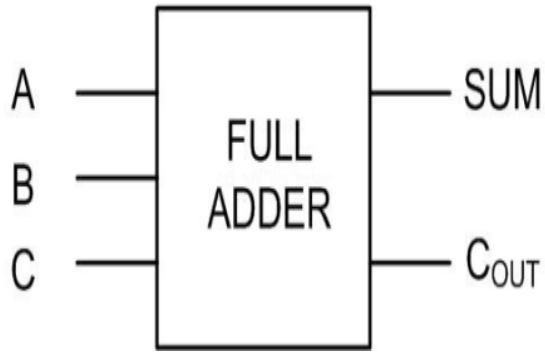

Fig. Block diagram of one-bit full adder.

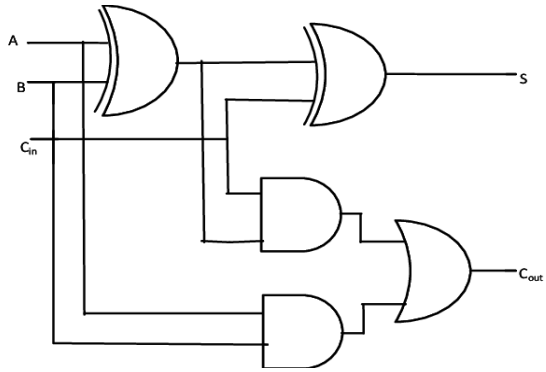

Fig. Logic diagram of one-bit full adder.

The gate level logical diagram of one- bit full adder has been shown in Fig.4 which uses the two X-OR gate for the sum, two AND gate and one OR gate for carry. The output of the two AND gate is used as an input of OR gate and the output of OR gate is providing the carry of one-bit full adder. Table I shows the truth table for full adder designed using CMOS based logic

FULLADDER TRUTH TABLE

Inputs			**Outputs**	
A	**B**	**C**	**Sum**	**Carry**
0	*0*	*0*	*0*	*0*
0	*0*	*1*	*1*	*1*
0	*1*	*0*	*1*	*0*
0	*1*	*1*	*0*	*1*
1	*0*	*0*	*1*	*0*
1	*0*	*1*	*0*	*1*
1	*1*	*0*	*0*	*1*
1	*1*	*1*	*1*	*1*

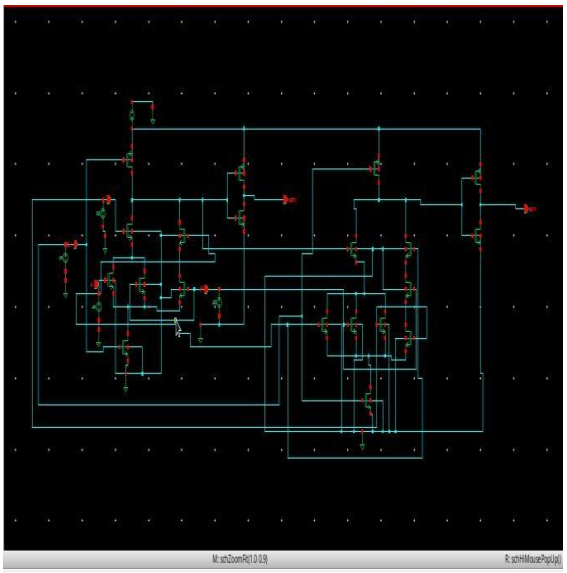

Fig. Schematic design of one-bit full adder which uses the Domino logic.

In this logic style we have used 4 *p*-MOS transistors and 16 *n*- MOS transistors. So there are a total 20 transistors being used

in designing the adder circuit by using Domino logic.

ONE- BIT FULL ADDER: RESULTS, DISCUSSION AND ANALYSIS: The analysis of one- bit full adder circuit is done using Cadence Virtuoso 6.1.7, 180nm technology. We have given the supply voltage 'vdc', 3V.

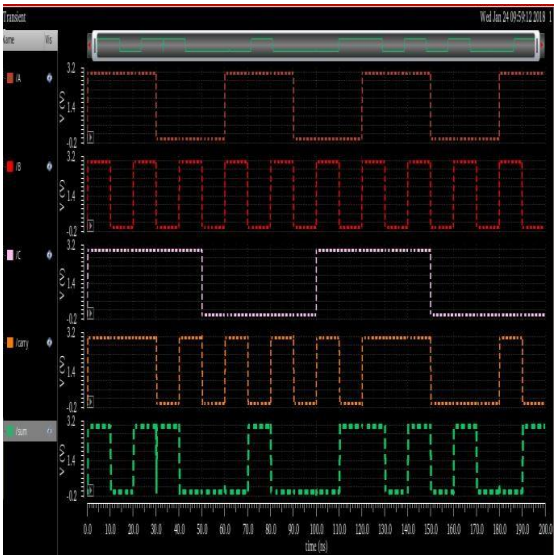

Fig. Simulated result of one-bit full adder based on CMOS logic.

We analysed the schematic of one-bit full adder circuit using Domino logic. Thereafter we verified the result for this logic with the truth table of full adder circuit as show in fig.9. When CLK is low p-mos will be on and it will charge the output node to Vdd, so we get the high output in this stage but we use an inverter for getting the output of adder so it will show both sum and curry low when the clk signal is low.

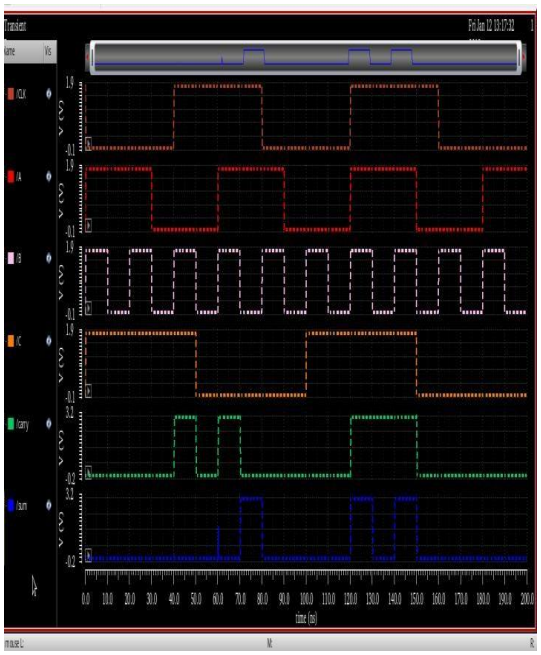

Fig. Simulated result of one-bit full adder using Domino logic

CONCLUSION

In this paper designing of full adder circuit using the CMOS logic and Domino logic has been done. We used Cadence Virtuoso 6.1.7 software, 180nm technology for analyzing the full adder circuit. It was found that Domino logic gives us very accurate results with less number of transistors and minimum delay as compare to the CMOS design logic. There are almost no glitches in Domino logic transient analysis. Further there is a decrease in chip area by 28.5% and delay by 47.37% in Domino logic as compared to CMOS logic. Further, as shown in the power graph of CMOS logic and Domino logic it was observe that instantaneous power is more in CMOS based logic as compare to the Domino logic so there are more chances of device failure in CMOS logic as compare to the Domino logic.

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