B4 INVERTER FED INDUCTION MOTOR WITH DC LINK VOLTAGE OFFSET SUPRESSION

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ABSTRACT

The main aim of this project is three phase nine level inverter fed induction motor drives for harmonic reduction in existing system The four-switch three-phase (B4) inverter, having a lower number of switches, was first presented for the possibility of reducing the inverter cost, and it became very attractive as it can be utilized in fault-tolerant control to solve the open/short-circuit fault of the six-switch three-phase (B6) inverter. However, the balance among the phase currents collapses due to the fluctuation of the two dc-link capacitor voltages; therefore, its application is limited. This paper proposes a predictive torque control (PTC) scheme for the B4 inverter-fed induction motor (IM) with the dc-link voltage offset suppression. The voltage vectors of the B4 inverter under the fluctuation of the two dc-link capacitor voltages are derived for precise prediction and control of the torque and stator flux. The three-phase currents are forced to stay balance by directly controlling the stator flux. The voltage offset of the two dc-link capacitors is modeled and controlled in the predictive point of view. In extension system we proposed nine level inverter fed induction motor drive. Compare to existing system proposed system is more efficient system for harmonic reduction as well as smoothing the wave shape.

Index terms: *Nine level inverter, Induction motor, predictive torque control (PTC), B4 inverter, harmonics*

I. INTRODUCTION

The four-switch inverters are known to have several disadvantages compared to normal six-switch inverters: the voltage utilization factor is halved compared to the six-switch inverter. On the other hand, the capacitor center tap voltage is fluctuating, and it destroys the balance among the motor phase currents . The capacitor center tap voltage fluctuation increases as the load torque becomes higher or the frequency of a B4 inverter becomes lower, and the unbalanced motor current leads to an inverter failure and torque pulsation [13]. In order to mitigate the effects of the capacitor center tap voltage fluctuation, several papers were published. An adaptive space vector modulation (SVM) approach was proposed to compensate the dc-link voltage ripple in a B4 inverter [12]. Kim *et al*. [13] investigated motor current unbalance from the perspective of source impedance and the voltage variation caused by the current flowing through the capacitor, and proposed a current distortion compensation scheme. Lee *et al*. [14] proposed a compensation method by adjusting switching times considering the capacitor center tap voltage fluctuation. Wang *et al*. [15] investigated the cause and effect of the capacitor center tap voltage fluctuation in analytical point of view, and the capacitor voltage offset was suppressed by employing certain switching states. However, the capacitor voltage offset suppression was

achieved at the expense of the B4 inverter's output performance. The works mentioned earlier were dedicated to obtain the balanced three-phase currents of the B4 inverter, but the flux and torque control was not considered. Regarding the flux and torque control of a B4 inverter-fed IM drive, several papers on closed-loop control scheme were published. Uddin *et al*. [16] discussed a closed-loop vector control scheme for a B4 inverter-fed IPM synchronous motor, in which the current loop was controlled by a hysteresis controller and the speed loop was controlled by a fuzzy-logic controller Kashif *et al*. [17] utilized a three-layer feed-forward back propagation artificial neural network for flux control of a B4 inverter fed IM drive. El Badsi *et al*. [18] used a DTC scheme for torque and flux control of a B4 inverter-fed IM drive. Unfortunately, the two capacitor voltages were assumed constant in these papers. In fact, as a result of one-phase current flows through the split dc-link voltage sources, the fluctuation will inevitably appear in the two capacitor voltages, which deteriorates the output performance of the B4 inverter (i.e., torque pulsation and unbalanced three-phase currents). More seriously, if the balanced condition of the currents flowing in the two capacitor voltages is corrupted, the two capacitor voltages will deviate in two opposite directions till shutting down of the B4 inverter. With the development of fast and powerful microprocessors, increasing attention has been dedicated to the use of model predictive control (MPC) in power electronics [19]. The first ideas about this strategy applied to power converters started in the 1980s [20], [21]. The main concept is based on calculating the system's future behavior to obtain optimal values for the actuating variables. With this intuitive concept, predictive control can be applied to a variety of systems, in which constraints and nonlinearities can be easily included, multivariable case can be considered, and the resulting controller is easy to implement [22]. These features render the approach very attractive and effective for the control of power electronics system [23], [24], including drive control [25]–[27], especially predictive torque control (PTC; particular for a two-level converter with horizon $N = 1$). In the PTC, the complete model and future behavior of the inverter-fed drives are taken into account. A cost function relating to torque and flux errors reduction is defined to evaluate the effects of each voltage vector and the one minimizing the cost function is selected [28]–[36]. In spite of the outstanding performance of B6 inverter-fed drives based on the PTC, PTC for B4 inverter-fed drives did not get many attentions to the researchers. Some simulation results of PTC for the B4 inverter-fed drives emulating the B6 case were carried out in [36]. However, the dc-link voltages fluctuation, which is the intrinsic feature of the B4 inverter, was not considered. Additionally, and the offset suppression of the two capacitor voltages was not mentioned. In this paper, the special issues on using the famous PTC control scheme for B4 inverter-fed IM drives are analyzed and discussed. Each half dc-link voltage is measured to achieve precise prediction and control of torque and stator flux. The voltage vectors of the B4 inverter under the fluctuation of the two dc link capacitor voltages are derived for precise prediction and control of the torque and stator flux. The closed-loop control of torque and stator flux is achieved by the cost function in the PTC. The balanced three-phase currents are achieved by controlling the stator flux well. The capacitor voltage offset is modeled and suppressed in the predictive point of view. The effectiveness of the proposed scheme is demonstrated by extensive simulation and experimental results. Because of the halved switch states corresponding to B6 one, the real-time implementation time cost for the PTC scheme in B4 inverter is reduced in a sampling period. This paper is organized as follows.

II MULTILEVEL INVERTER

An **inverter** is an electrical device that converts direct current (DC) to alternating current (AC); the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits. Static inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utility high-voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries. The electrical inverter is a high-power electronic oscillator. It is so named because early mechanical AC to DC converters was made to work in reverse, and thus was "inverted", to convert DC to AC. The inverter performs the opposite function of a rectifier

Cascaded H-Bridges inverter

A single-phase structure of an m-level cascaded inverter is illustrated in Figure 31.1. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. An example phase voltage waveform for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure 31.2. The phase voltage $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$.

For a stepped waveform such as the one depicted in Figure 31.2 with s steps, the Fourier Transform for this waveform follows

$$V(\omega t) = \frac{4V_{dc}}{\pi}\sum_{n}\left[\cos(n\theta_1)+\cos(n\theta_2)+\ldots+\cos(n\theta_s)\right]\frac{\sin(n\omega t)}{n}, \quad \text{where } n = 1, 3, 5, 7, \ldots$$

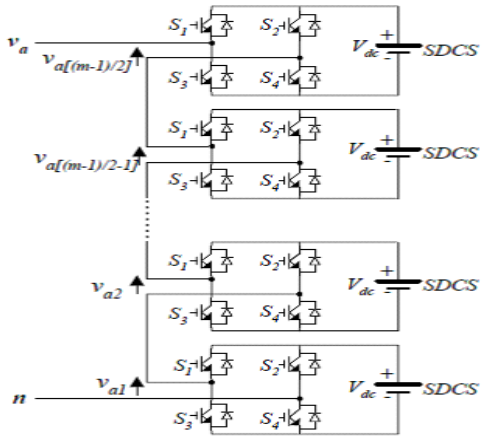

FIG 1.Single-phase structure of a multilevel cascaded H-bridges inverter

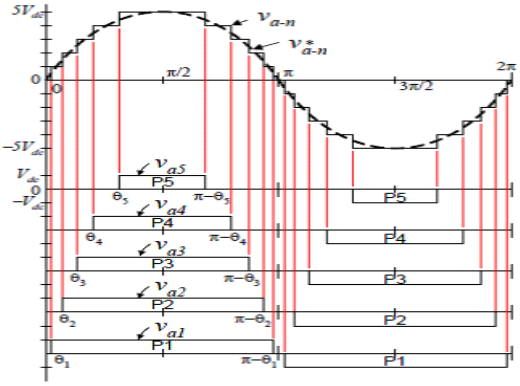

FIG 2.Output phase voltage waveform of an 11-level cascade inverter with 5 separate dc sources.

III. OPEARTING PRINCEPLE OF EXISTING SYSTEM

The B4 topology consists of a two-leg inverter, as illustrated in Fig. The dc-link is split into two voltage sources, to the middle of which one load phase is connected. For convenient analysis, the inverter is considered for implementation by ideal switches (T1–T4) (i.e., with no dead time and no saturation voltage drop). This means, the switching states of leg b (T1–T2) and leg c (T3-T4) can be denoted as binary states variables *Sb* and *Sc*. To prevent the short circuit of the dc-link, the simultaneous closed states of two switches in each leg are usually forbidden. Therefore, a binary "1" will indicate the close state of the upper switch, whereas a binary "0" will indicate the close state of the lower switch.

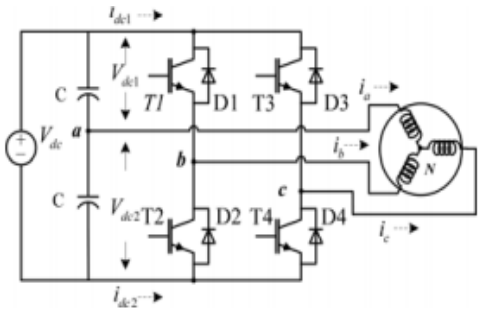

Fig.3. Circuit diagrams of a B4 inverter-fed induction motor drive

The basic voltage vectors can be defined according to the switching states. Assume that the three-phase voltages are balanced, the phaseto-neutral voltages *VaN* ,*VbN* ,*VcN* are given as follows:

$$\begin{aligned} V_{aN} &= \tfrac{V_{dc1}}{3}(-S_b - S_c) + \tfrac{V_{dc2}}{3}(2 - S_b - S_c) \\ V_{bN} &= \tfrac{V_{dc1}}{3}(2 \cdot S_b - S_c) + \tfrac{V_{dc2}}{3}(2 \cdot S_b - S_c - 1) \\ V_{cN} &= \tfrac{V_{dc1}}{3}(2 \cdot S_c - S_b) + \tfrac{V_{dc2}}{3}(2 \cdot S_c - S_b - 1) \end{aligned} \quad (1$$

where *V*dc1 and *V*dc2 are the upper and the lower dc-link capacitor voltages, respectively.

Considering all the possible combinations of (*Sb*, *Sc*), phaseto-neutral voltages values are given in Table I. The Clarke transform applied to the stator voltages yields as follows:

$$\begin{bmatrix} V_{\alpha s} \\ V_{\beta s} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{bmatrix}$$

Where the *Vαs* and *Vβs* are the *α*- and *β*-axis stator voltage, respectively. The voltage vectors are expressed by - → *us* = *Vα* + *j*∗*Vβ* . Therefore, the four active voltage vectors (*V*1 to *V*4) in the *αβ* plane are given in Table II. It is clearly revealed that in Table II, the B4 inverter can only produce four basic nonzero voltage vectors. The basic voltage vectors change in amplitude and angle in case of dc-link voltage are not equal.

IV.OPEARTING PRINCEPLE OF PROPOSED SYSTEM

Block diagram of 9-level three phase inverter fed induction motor drive is shown in Fig. 10. The induction motor is connected to a nine level inverter for harmonic mitigation as shown THD in fig 15.

V SIMULATION RESULTS

EXISTING RESULTS

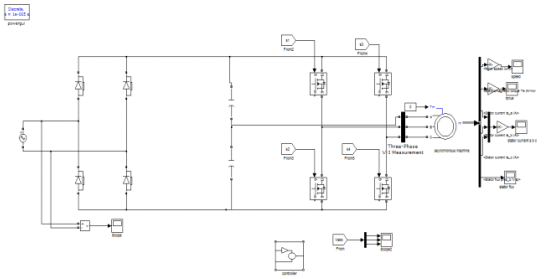

Fig 4. matalab/simulink diagram of existing model

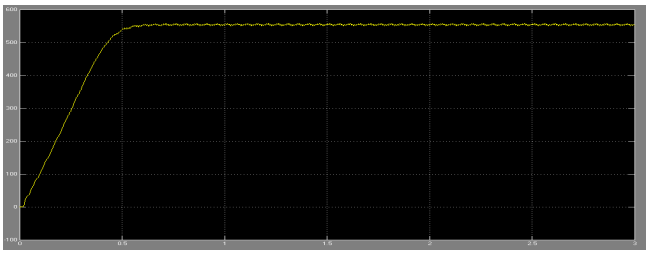

Fig 5 . speed

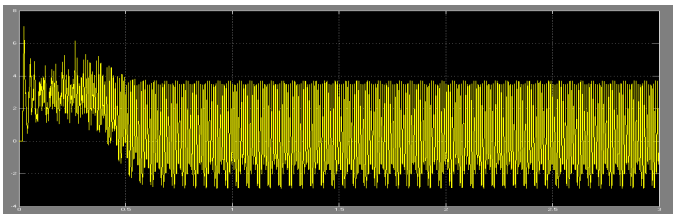

Fig 6. Torque

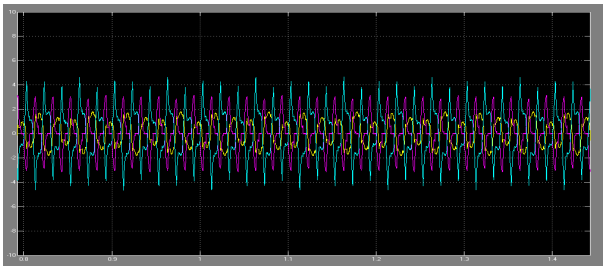

Fig 7. Stator cureent

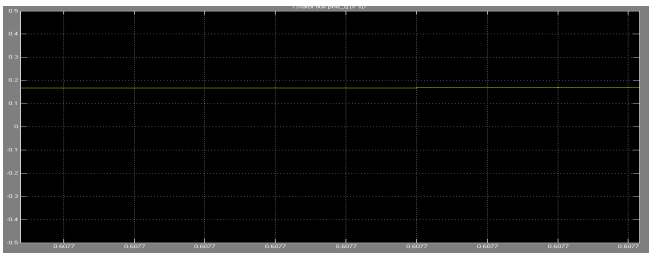

Fig 8 . flux

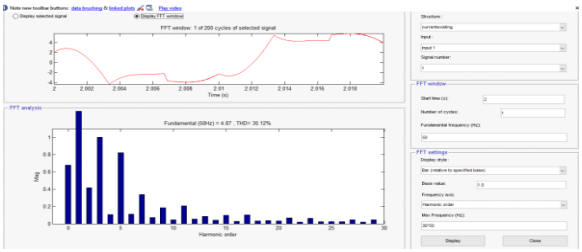

Fig 9. Inverter output current THD % .

EXTENSION RESULTS

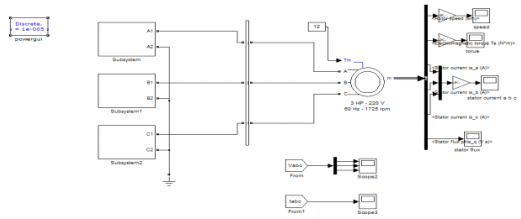

Fig 10. MATLAB/SIMULINK diagram of proposed nine level inverter fed induction motor drive

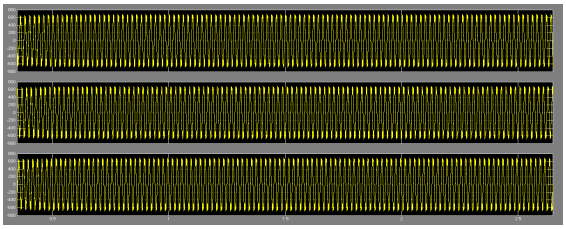

Fig 11 . out put voltage of nine level inverter

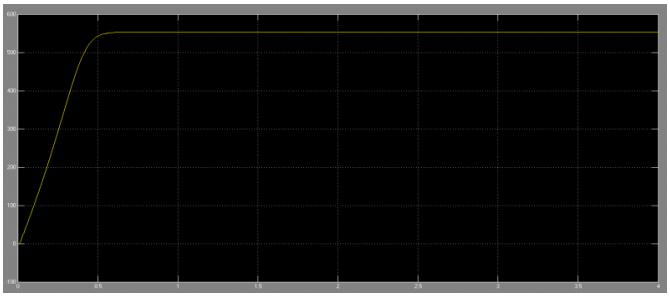

fig 12. Speed

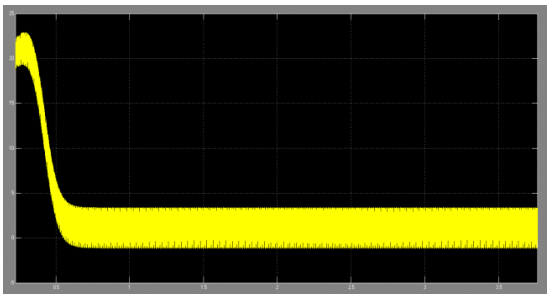

Fig 13 . Torque

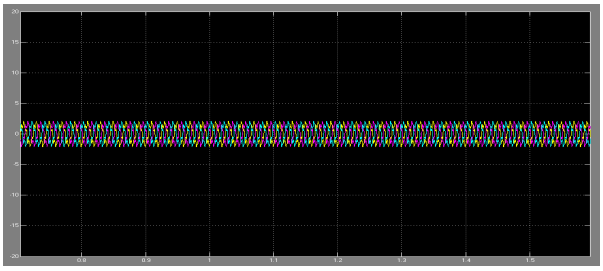

Fig 14 .stator current

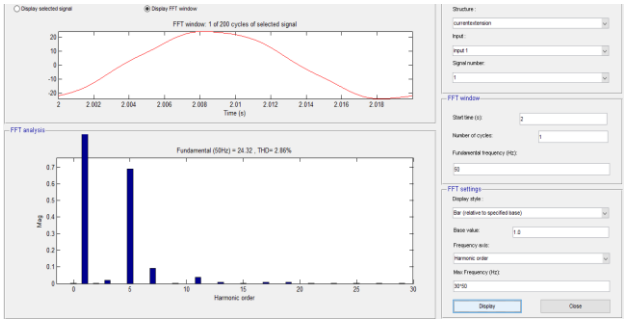

Fig 15 . Inverter output Current THD%

VI CONCLUSION

In this paper, the special issues on using the famous PTC control scheme for a B4 inverter-fed IM drives are analyzed and discussed. The voltage vectors of the B4 inverter under the fluctuation of the two dc-link capacitor voltages are derived for precise prediction and control of the torque and stator flux. The balanced three-phase currents are achieved and the capacitor voltage offset is suppressed in the proposed scheme. The theory, design, and performance evaluation of the proposed scheme for the B4 inverter-fed IM drive are investigated. The proposed B4 inverter-fed IM drive has been found acceptable for high performance industrial variable-speed-drive applications considering its cost reduction and other inherent advantageous features. Certainly, the additional work is still remained to develop more efficient PTC scheme and answers the remaining questions: the robustness toward parameter deviation, parameter sensitivity of this scheme, for the parameter values may vary in the motor drives, while in other cases it is difficult to get a precise value of the parameters. In extension model we proposed nine level inverter fed induction motor drive. Considering extension system is more sufficient compare to B4 inverter for harmonic reduction.

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