PULSED LATCHES BASED LOW POWER AND AREA EFFICIENT SHIFT REGISTERS

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Abstract
Shift Registers are building blocks used for the storage of data in many devices. Currently, Flip flops which have been used in Shift Registers consume more Power and impose a heavy load on Clock distribution networks. The Proposed work overcomes the Power consumption and reduces the delay by using the Pulsed Latches instead of the Flip flops. Conventional Latches-Static differential Sense Amplifier Shared Pulse Latch (SSASPL) has been used where the number of Transistors has been reduced. Trigger generator is used to give non overlap clock signals to the memory elements, which reduced the delay and produced the fast implementation of the data. There is a high demand for minutely packed power devices that have higher efficiency of area which has lead the industry of VLSI to venture into the unknown. As technology moves into these levels the power management requirement of the devices rise. This paper proposes allow power and area-efficient shift register using pulsed latches. The area and power consumption are made to reduce by substituting flip-flops with pulsed latches.

Keywords*: area efficient, pulsed clock generator, pulsed latch, shift register, flip-flop.*

INTRODUCTION:

Technology has invaded into the life of human beings to such deep extent that today everyone has a wish for smaller faster fancier gadgets. This wish has been granted to them by the technological developments in the field of VLSI technology. A SHIFT register is the basic building block in a VLSI circuit. Shift registers find them to be use full commonly in many applications, such as digital filters, communication receivers, and image processing ICs. Now a days, as there is high demand of images with utmost clarity the size of the image data continues to increase, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register. A 16-megapixel CMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations.

Shift Register is the building block in many VLSI circuits. Shift Registers are commonly used in many applications. Such as digital filters,[2] communication receivers[3] and image processing ICs.[6] Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the Shift Register increases to process large image data in image processing ICs. As the word

length of the Shift Register increases, the area and Power consumption of the Shift Register also increases. The Power dissipation is an important factor for many applications. The optimization Techniques of Power are used at different levels of digital design. The architecture of the Shift Register is simple. An N-bit Shift Register is composed of series of connected N data Latches. The smallest Latch is suitable for the Shift Register to reduce the area and Power consumption. Recently, Pulsed Latches have replaced the Flip flops in many applications, because a pulsed Latch is much smaller than a Flip flops.[1]

Proposed Architecture

A master-slave flip-flop using two latches in Fig.1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1(b). All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption. The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. 2. The shift registers in Fig. 2(a) consists of several latches and a pulsed clock signal (CLK_pulse). The operation waveforms in Fig. 2(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signals of the first latch (IN) is constant during the clock pulse width (TPULSE). But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

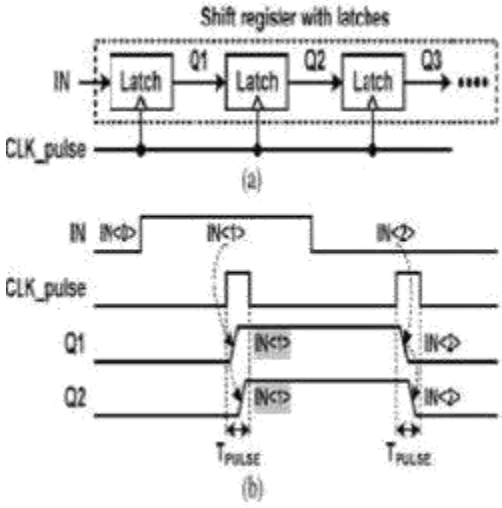

Fig. 2. Shift register with latches and a pulsed clock
signal. (a) Schematic. (b)Waveforms

One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 3(a). The output signal of the latch is delayed and reaches the next latch after the clock pulse. As shown in Fig. 3(b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 3(a). The output signal of the latch is delayed and reaches the next latch after the clock pulse. As shown in Fig. 3(b) the

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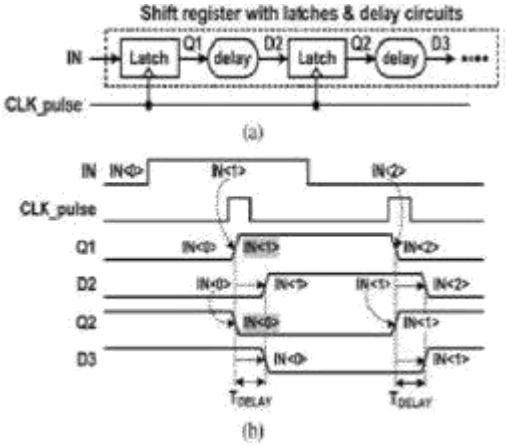

Fig. 3. Shift register with latches, delay circuits, and a pulsed clock signal. (a)Schematic. (b)Waveforms

Power optimization: The power optimization is
similar to the area optimization. The power is consumed mainly in latches and clock-pulse circuits. Each latch consumes power for data transition and clock loading. When the circuit powers are normalized with a latch, the power consumption of a latch and a clock-pulse circuit
are1 and , respectively. The total power consumption is also
$\{\alpha_p \times (K+1) + N\left(1+\frac{1}{K}\right)\}$ .An integer for the minimum power is selected as a divisor of , which is nearest to
$\sqrt{N/\alpha_p}$.

Chip Implementation: The maximum clock frequency in the conventional shift register is limited to only the delay of flip-flops because there is no delay between flip-flips. Therefore, the area and power consumption are more important than the speed for selecting the flip-flop. The proposed shift register uses latches instead of flipflops to reduce the area and power consumption.

4. RESULTS

Thus the proposed Shift Register reduces the power and the number of delayed pulsed clock signals. Thus an inverter, buffer, AND gate, delay circuit, Latches, Shift register have been implemented in 0.18µm process.fig.7. represents the SSASPL-latch waveform implemented in 0.18µm process.

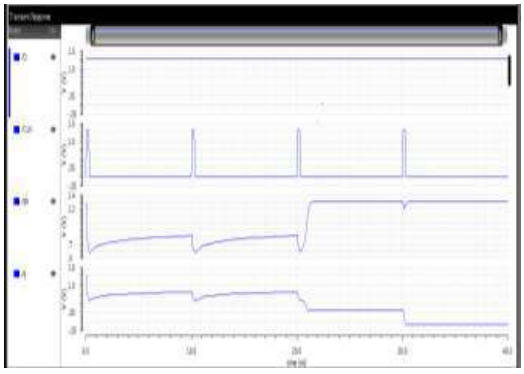

Fig.7. Latch circuit waveform
The latch produced the transparent signal from D input to Q output.

Pulsed clock generator

The Pulsed clock generator circuit is implemented in a 0.18µm process. Fig. 8 represents the Pulsed clock generator waveform. For every clock, the clock pulses clk1, clk2, clk3, clk4 have been analysed with delay.

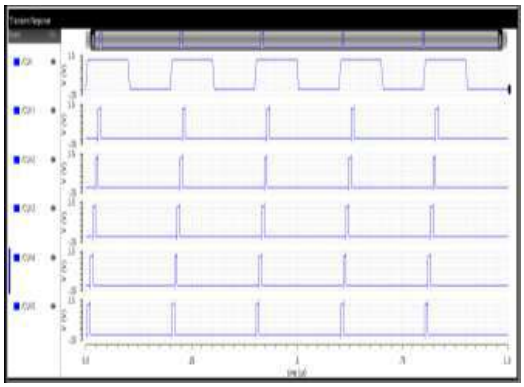

Fig.8. Pulsed clock generator waveform

CONCLUSION

This paper proposed a low-power and area-efficient shift register using pulsed latches. The shift register reduces area and power consumption by substituting flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals as an alternative of a single pulsed clock signal.

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