CONSTRUCTING THE BLUE PRINT OF RAPID REVERSE CONVERTER THROUGH THE PARALLEL PREFIX ADDER

N.SOWJANYA
PG Scholar,
Dept. of ECE,
Chadalawada Ramanamma
Engineering College,
Tirupathi, A.P.
E-Mail: nallabathini.sowji@gmail.com

DR.V.THRIMURTHULU
Professor,
Dept. of ECE,
Chadalawada Ramanamma
Engineering College,
Tirupathi, A.P.
E-Mail: vtmurthy.v@gmail.com

MS.G.DILLIRANI
Assistant professor,
Dept. of ECE,
Chadalawada Ramanamma
Engineering College,
Tirupathi, A.P.
E-Mail: gdillirani@gmail.com

ABSTRACT

In this project, the analysis of residue number system reverse converters using the well-known regular and modular parallel pre-fix adders is presented. The VLSI implementation reduces delay and improves area×time^2, at the cost of increased power consumption, which is the major cause for preventing the use of parallel-prefix adders to achieve high-speed reverse converters in nowadays systems. Thus, the problem of higher power consumption is solved by designing reverse converter using parallel pre-fix adder components which provide better tradeoffs, between delay and power consumption. In this work a new technique is proposed to design and implement the reverse converter which helps the designer to improve the performance of the reverse converter based on the target application and existing constraints. Numerous reverse converters for different moduli sets already existed, which can be categorized into three types. The first ype consists of converters with a tree of CSAs with EAC followed by a two-operand modulo 2k −1 CPA. A second type includes complex reverse converters, which have several CSAs and CPAs with EACs followed by a final regular subtractor with two operands of different size. The implementation of this subtractor using regular binary-adder results in one operand with some constant bits. The third type covers the reverse converters that have been designed for moduli sets with moduli other than the popular 2n and 2n ± 1. Hence a new technique is developed for the first and second types of reverse converters for applying the HMPE and HRPX in the reverse converter design is realized in VHDL. The power consumption values are calculated using TSMC 65-nm CMOS.

Index Terms—*Digital arithmetic, parallel-prefix adder, residue number system (RNS), reverse converter.*

1.INTRODUCTION

In the world of battery-based and portable devices, the residue number system (RNS) can play a significant role due to its low-power features and competitive delay. The RNS can provide carry-free and fully parallel arithmetic operations for several applications, including digital signal processing and cryptography. However, its real usage requires forward and reverse converters to be integrated in the existing digital systems. The reverse conversion, i.e., residue to binary conversion, is a hard and time-consuming operation. Hence, the problem of designing high-performance reverse converters has motivated continuous research using two main approaches to improve the performance of the converters: 1) investigate new algorithms and novel arithmetic formulations to achieve simplified conversion formulas and 2) introduce new module sets, which can lead to more simple formulations. Thereafter, given the final simplified conversion equations, they are computed using well-known adder architectures, such as carry-save adders (CSAs) and ripple-carry architectures, to implement carry-propagate adders (CPAs) and, more seldom, fast and expensive adders such as the ones with carry-look ahead or parallel-prefix architectures.

In this brief, for the first time, we present a comprehensive methodology to wisely employ parallel-prefix adders in carefully selected positions in order to design fast reverse converters. The collected experimental results based on area, delay, and power consumption show that, as expected, the usage of the parallel-prefix adders to implement converters highly increases the speed at the expense of additional area and remarkable increase of power consumption. The significant growing of power consumption makes the reverse converter not competitive. Two power-efficient and low-area hybrid parallel-prefix adders are presented in this brief to tackle with these performance limitations, leading to significant reduction of the power delay product (PDP) metric and considerable improvements in the area-time2 product (AT2) in comparison

with the original converters without using parallel-prefix adders.

II EXISTING METHOD

The Chinese remainder theorem, or other related improved approaches and techniques underlie the RNS reverse conversion, whose formulation can be directly mapped to ripple-carry adders (RCA). However, this leads to significant speed degradation, due to the linear increase of the delay in the RCA with the number of bits. Parallel-prefix adders can be used in the RNS reverse converters to bind the delay to logarithmic growth. However, in reverse converters, several parallel-prefix adders are usually required.

Even when only one adder is used, the bit length of this adder is quite large. Consequently, this results in high power consumption notwithstanding its high speed. Therefore, in this section, two approaches that take advantage of the delay properties of the parallel prefix adders with competitive power consumption are introduced.

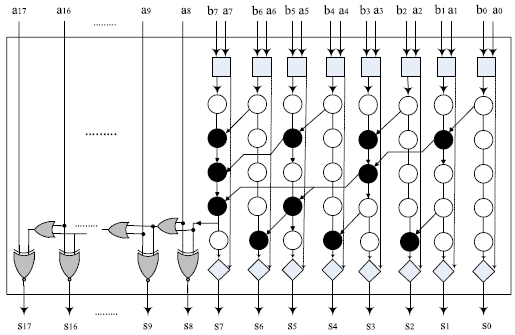

Figure 1: HRPX structure with BK prefix network

Usually, one regular binary addition is required in reverse converter structures to achieve the final binary representation. This final addition has an important effect in the total delay of the converter due to the large bit-length of the operands. A thorough assessment of this final regular addition in recent converter designs shows that one of the operands has some constant bits with value 1 as highlighted by the following lemma, which applies to a class of converters described.

Lemma 1: ($2n + 1$) bits of the second operand of CPA4 of the converter in [10] are always constant and equal to one's.

Proof: The [10, CPA4] is a ($4n + 1$)-bit regular RCA that performs the subtraction presented in [10, eq. (52)]. This subtraction is accomplished in [10] as follows:

$$S = P - T = P + \overline{T} + 1$$

where P and T are $4n + 1$ and $2n + 1$ bits binary vectors, respectively.

Based on the Lemma 1, a regular parallel-prefix adder with the desirable prefix structure can be used to perform the first part of the addition, for which the corresponding bits of the operands are fully variable, and a RCA with simplified logic to do the second part (full adder becomes XNOR/OR gates because of the constant operand). The proposed hybrid regular parallel-prefix XOR/OR (HRPX) adder component to perform the ($4n + 1$)-bit addition of CPA4] for $n = 4$ is shown in Fig. 1. It should be noticed that due to the architecture of the reverse converter, the carry output of the XNOR/OR chain is not needed and can be ignored.

Second, the modulo $2n - 1$ addition is an essential operation in the reverse conversion for most moduli sets. The regular CPA with end around carry (EAC) is by default a moduli$2n - 1$ adder with double representation of zero, but in reverse converters a single representation of zero is required. So, a one detector circuit has to be used to correct the result, which imposes an additional delay. However, there is a binary-to-excess-one converter (BEC) , which can be modified to fix the double-representation of zero issue.

The main reason for the high power consumption and area overhead of these adders is the recursive effect of generating and propagating signals at each prefix level. An optimized approach is proposed in, which uses an extra prefix level to add the output carry. However, this method suffers from high fan-out, which can make it usable only for small width operands. However, we could address this problem by eliminating the additional prefix level and using a modified excess-one unit instead.

In contrast to the BEC, this modified unit is able to perform a conditional increment based on control signals as shown in Figure 3.2, and the resulted hybrid modular parallel-prefix excess-one (HMPE) adder is depicted in Figure 3.3.

The HMPE consists of two parts: 1) a regular prefix adder and 2) a modified excess-one unit.

First, two operands are added using the prefix adder, and the result is conditionally incremented afterward based on control signals generated by the prefix section so as to assure the single zero representation.

Summarizing, the HMPE is highly flexible, since it can be used with every prefix networks. Hence, the circuit

performance metrics such as area, delay, and power-consumption can be adjusted by selecting the desired prefix structure. On the other hand, the HRPX avoids the usage of a large size parallel-prefix adder with high power consumption, and also does not have the penalty of using the long carry-propagation chain of a RCA.

III PROPOSED METHOD

Reverse converter design methodology

In this section, the methodology of reverse converter design is described. In the following, a method employing distinct components in the architecture of the reverse converter will be presented. Several reverse converters for different moduli sets have been introduced, which can be classified into three classes.

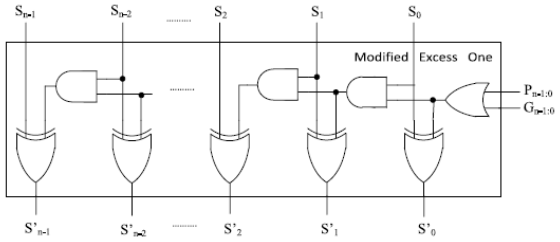

Figure 2: Modified excess-one unit

The first class consists of converters with a tree of CSAs with EAC followed by a two-operand modulo $2k - 1$ CPA. A second class includes more complex reverse converters, which have several CSAs and CPAs with EACs followed by a final regular subtractor with two operands of different size. The implementation of this subtractor using regular binary-adder results in one operand with some constant bits. The third class covers the reverse converters that have been designed for moduli sets with moduli other than the popular $2n$ and $2n \pm 1$.

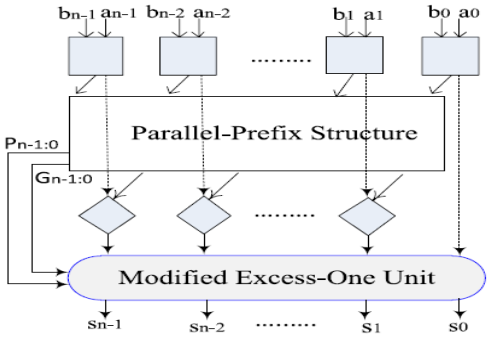

Figure 3: HMPE structure

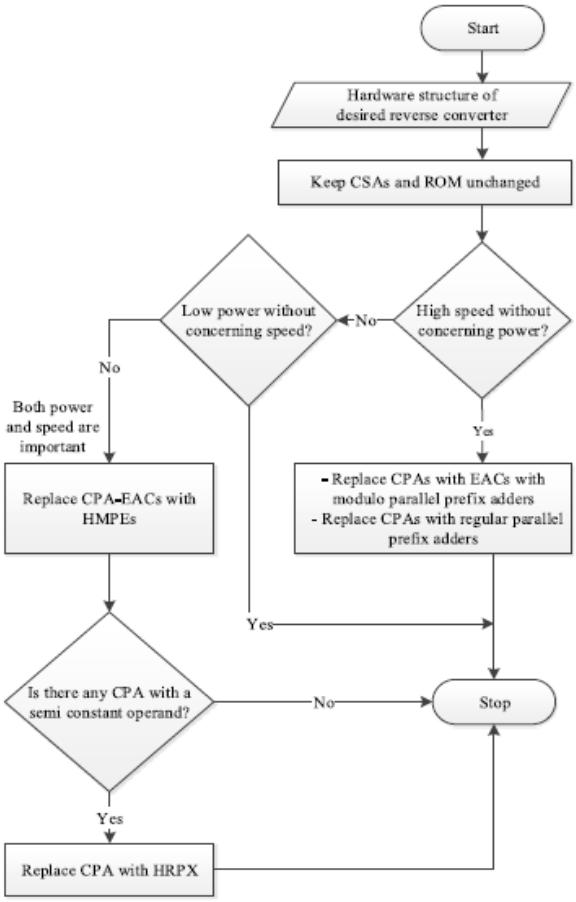

Figure 4: Reverse converter design methodology

In the following, we describe a methodology for designing reverse converters in the first and second classes. The suggested method for applying the HMPE and HRPX in the reverse converter is shown in Fig 4.

First of all, it is relevant to decide about the required performance metrics based on the specified application. If it is just important to achieve the least power consumption and hardware cost without considering speed, no prefix adder is needed. On the other hand, if high speed is the designer goal, the CPAs with EAC and the regular CPAs should be replaced by traditional parallel prefix modulo $2n - 1$ adders and regular parallel-prefix adders, respectively. However, for the VLSI designers, a suitable tradeoff between speed, power, and area is often more important. In this case, first, CPAs with the EAC can be replaced by the HMPEs. Then, if the converter contains a regular CPA where one of its operands has a string of constant bits with the value of one, it can be replaced with the HRPX.

VLSI implementations

In order to support a thorough assessment, especially for power consumption, the proposed method was applied to three different reverse converters and application-specific integrated circuits (ASICs) were implemented. The target reverse converters are: 1) the Converter-1 for moduli set $\{2n - 1, 2n, 2n+1, 22n+1 - 1\}$; 2) the Converter-2 for $\{2n - 1, 2n+1, 22n, 22n+1 - 1\}$; and 3) the Converter-3 for $\{2n - 1, 2n+1, 22n, 22n+1\}$.

The implemented converters can be classified as follows: 1) cost effective designs using only the RCAs for the CPAs with the EAC and regular CPAs; 2) speed efficient designs, which substitute all the CPAs with EAC and the regular CPA by the parallel-prefix modulo $2n - 1$ adders of [22]-Type-I, and KS regular parallel-prefix adders, respectively; and 3) designs that use both HMPE and HRPX, tradeoff between circuit parameters. Three well-known approaches for prefix network, i.e., Brent–Kung (BK), SK, and KS, have been considered for implementing the required prefix network in the proposed designs.

The circuits for all these configurations were designed and specified in the VHDL. Structural or behavioral descriptions can be considered. Behavioral VHDL describes just the circuit operation, and therefore the circuit's quality depends on synthesis tool. However, herein our purpose is to compare the proposed architectures on a fair basis, and independently of the particular abilities of the synthesis tools. Consequently, a structural VHDL description is adopted. After a thorough verification, the ASICs were implemented using a general purpose standard cell library (TCBN65GPLUS, version 200A) tailored for the TSMC 65-nm CMOS logic salicide process (1-poly, 9-metal).

The Cadence RTL Compiler tools (version v09.10-s242_1) was used for synthesizing the design and the Cadence Encounter and Nano Route tools (versions v09.12-s159 and v09.12-s013, respectively) for placing and routing. Note that in any of the aforementioned technologies, no manual optimization of any kind was introduced. In addition, four different values of n (4, 8, 12, and 16) were considered to obtain experimental results for the different configurations of the implemented converters. The obtained results are presented in Tables I–VI. The results include: chip area (square micrometer), useful area (square micrometer), delay (nanosecond), power (milliwatts), AT2, and PDP. The AT2 and PDP are used to compare the circuit's area/latency and power/latency balancing.

The suggested designs have considerably improved the delay, AT2, and PDP while slightly increasing the area. Although, more power was consumed, the balance between power and delay becomes more competitive when the PDP metric is adopted. By comparing with the converter using fully parallel-prefix adders, the area, power, AT2 (except at $n = 4$), and PDP of the proposed designs are significantly improved, but the delay increases. Similar behavior is observed except for the PDP metric. The PDP for the proposed converters are worse than for the RCA based in three cases, but this improves for larger values of n, even for $n = 16$ the HMPE and HRPX-SK structure has better PDP than the RCA-based one.

Finally, the practical interest of the proposed approaches can be verified in Tables V and VI. Our main goal is to decrease the designs. In the other hand, the proposed designs consume more power to achieve higher speed than the RCA-based ones.

Summarizing, the use of modular and regular parallel-prefix adders proposed in this brief in reverse converters highly decrease the delay at the expense of significantly more power and circuit area, whereas the proposed prefix-based adder components allows one to achieve suitable tradeoffs between speed and cost by choosing the right adders for the parts of the circuits that can benefit from them the most.

Advantages

- The HMPE is highly flexible, since it can be used with every prefix networks.
- The circuit performance metrics such as area, delay and power consumption can be adjusted by selecting the devices prefix structure.
- The HRPX avoids the usage of a large size parallel prefix adder with high power consumption and also does not have the penalty of using the long carry propagation chain of a RCA.
- Low power dissipation
- High speed
- Least hardware cost

Applications

- MAC unit
- Filters
- Arithmetic units
- Reversible logic

IV EXPERIMENTAL RESULTS

The Xilinx synthesis results of Hybrid Regular Parallel Prefix Adder (HRPX) structure with BK prefix network and Hybrid Modular Parallel Prefix Excess-One (HMPE) structure will be shown in figures respectively.

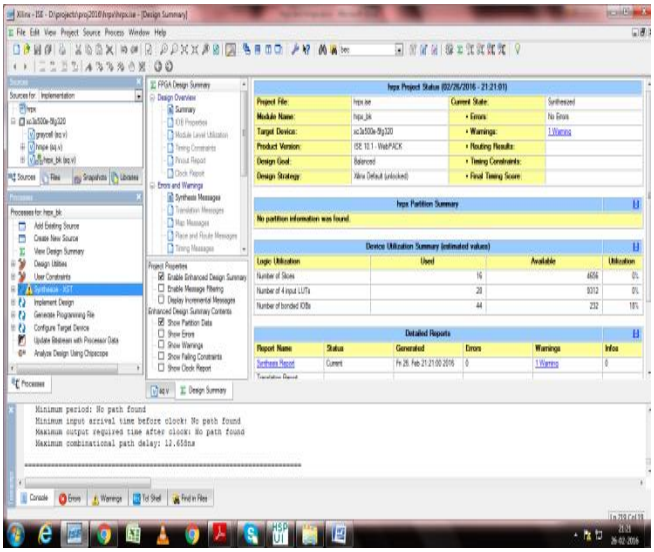

Figure 4.1: Hybrid Regular Parallel Prefix Adder (HRPX) structure with BK prefix network

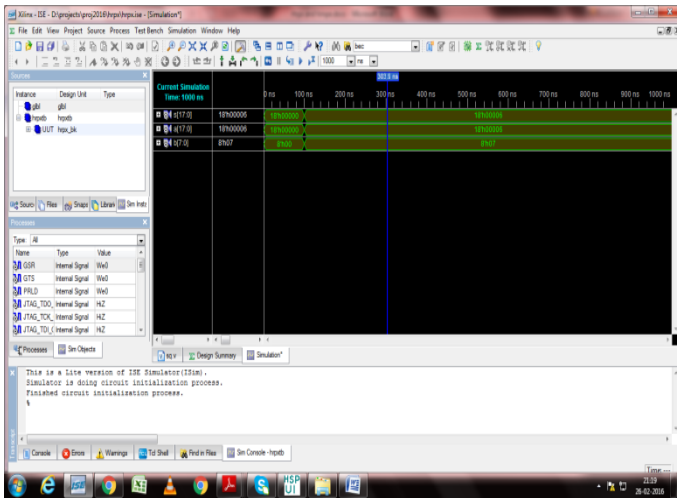

Figure 4.2: Simulation of Hybrid Regular Parallel Prefix Adder (HRPX) structure with BK prefix network

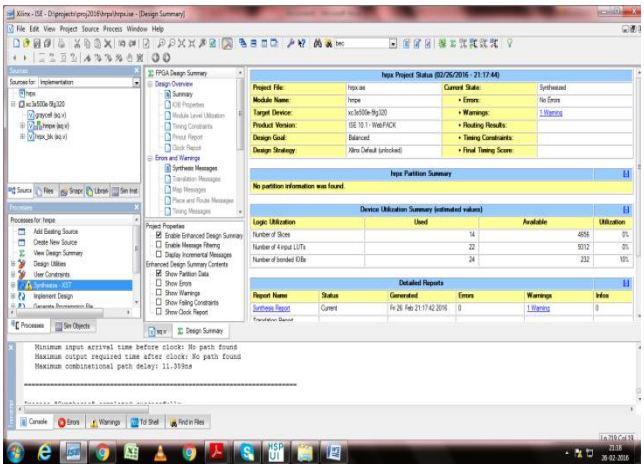

Figure 4.3: Hybrid Modular Parallel Prefix Excess-One (HMPE) structure

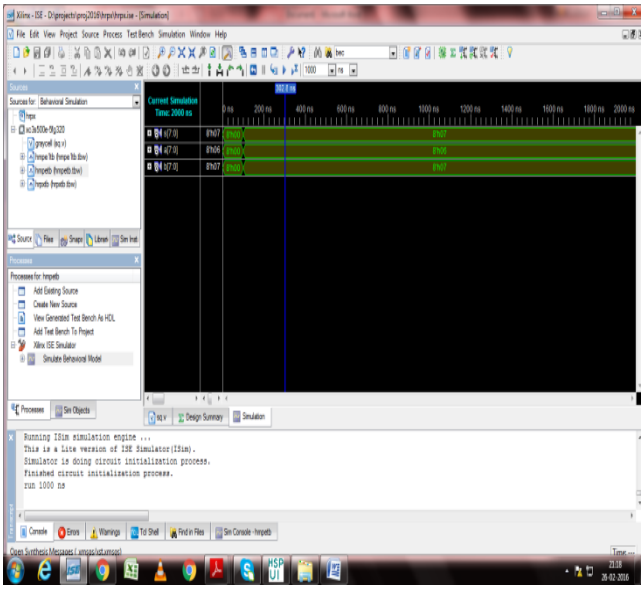

Figure 4.4: Simulation of Hybrid Modular Parallel Prefix Excess-One (HMPE) structure

Table 1: Comparison between HRPX, HMPE structure

Logic utilization	HRPX structure	HMPE structure
Number of slices	16	14
Number of 4 input LUTS	28	22
Number of bounded IOBs	44	24
Delay	12.66nsec	11.36nsec

V CONCLUSION AND FUTURE SCOPE

This proposed method that can be applied to most of the current reverse converter architectures to enhance their performance and adjust the cost/performance to the application specifications. Furthermore, in order to provide the required tradeoffs between performance and cost, new parallel-prefix-based adder components were introduced. These components are specially designed for reverse converters. Implementation results show that the reverse converters based on the suggested components considerably improve the speed when compared with the original converters, which do not use any parallel-prefix adder, and reduce the power consumption compared with the converters that exclusively adopt parallel-prefix adders.

ACKNOWLEDGMENT

We would like to thank Ms.G.Dillirani, for her outstanding support and also we would like to express gratitude Dr.V.Thrimurthulu for his technical advices.

REFERENCES

[1] A. Omondi and B. Premkumar, Residue Number Systems: Theory and Implementations. London, U.K.: Imperial College Press, 2007.

[2] B. Parhami, Computer Arithmetic: Algorithms and Hardware Designs,2nd ed., New York, NY, USA: Oxford Univ. Press, 2010.

[3] J. Chen and J. Hu, "Energy-efficient digital signal processing via voltage over scaling-based residue number system," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 21, no. 7, pp. 1322–1332, Jul. 2013.

[4] C. H. Vun, A. B. Premkumar, and W. Zhang, "A new RNS based DA approach for inner product computation," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 60, no. 8, pp. 2139–2152, Aug. 2013.

[5] S. Antão and L. Sousa, "The CRNS framework and its application to programmable and reconfigurable cryptography," ACM Trans. Archit. Code Optim., vol. 9, no. 4, p. 33, Jan. 2013.

[6] A. S. Molahosseini, S. Sorouri, and A. A. E. Zarandi, "Research challenges in next-generation residue number system architectures," in Proc. IEEE Int. Conf. Comput. Sci. Educ., Jul. 2012, pp. 1658–1661.

[7] K. Navi, A. S. Molahosseini, and M. Esmaeildoust, "How to teach residue number system to computer scientists and engineers," IEEE Trans. Educ., vol. 54, no. 1, pp. 156–163, Feb. 2011.

[8] Y. Wang, X. Song, M. Aboulhamid, and H. Shen, "Adder based residue to binary numbers converters for (2n − 1, 2n, 2n + 1)," IEEE Trans. Signal Process., vol. 50, no. 7, pp. 1772–1779, Jul. 2002.

[9] B. Cao, C. H. Chang, and T. Srikanthan, "An efficient reverse converter for the 4-moduli set {2n − 1, 2n, 2n + 1, 22n + 1} based on the new Chinese remainder theorem," IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 50, no. 10, pp. 1296–1303, Oct. 2003.

[10] A. S. Molahosseini, K. Navi, C. Dadkhah, O. Kavehei, and S. Timarchi, "Efficient reverse converter designs for the new 4-moduli sets {2n − 1, 2n, 2n + 1, 22n+1 − 1} and {2n − 1, 2n + 1, 22n, 22n + 1} based on new CRTs," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 4, pp. 823–835, Apr. 2010.

AUTHOR's PROFILE

N Sowjanya received her B.Tech degree in Electrical and Electronics Engineering from Indira priyadarshini college of engineering & technology for women, Kurnool (A.P), India, in the year 2012. Currently pursuing her M.Tech degree in VLSI Stream at Chadalawada Ramanamma Engineering College,Tirupati(A.P), India.. Her area of research Includes in Constructing the Blue Print of Rapid Reverse Converter through the Parallel Prefix Adder.

DR.V.THRIMURTHULU M.E., Ph.D., MIETE., MISTE Professor & Head of ECE Dept. He received his Graduation in Electronics & Communication Engineering AMIETE in 1994 from Institute of Electronics & Telecommunication Engineering, New Delhi, Post Graduation in Engineering M.E specialization in Microwaves and Radar Engineering in the year Feb, 2003, from University College of Engineering, Osmania University, Hyderabad., and his Doctorate in philosophy Ph.D from central University, in the year 2012. He has done his research work on Ad-Hoc Networks.

Ms.G.Dillirani is currently working as Assistant Professor in the Department of Electronics & Communication Engineering at Chadalawada Ramanamma Engineering College, Tirupati, India .She has 7 years of teaching experience. Her's extensive education includes B.Tech from SIET Puttur, University, plus M.Tech in SIET Puttur, A.P, India. from JNTU Hyderabad. She is making research in the field of Biomedical Signal Processing.