A HIGH EFFICIENT CONDITIONAL FEEDTHROUGH PULSED FLIP-FLOP FOR HIGH-SPEED APPLICATIONS

Sadanandappa N.
Sl. Gr. Lecturer
TMAES Polytechnic
Hosapete
sadanandanittur@gmail.com

Abstract

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. So this Low Power Pulse Triggered Flip Flop reviews various strategies and methodologies for designing low power circuits and systems. Pulse triggered FF (P-FF) is a single- latch structure which is more popular than the conventional transmission gate (TG) and master– slave based FFs in high-speed applications. Flip-flops and latches are the most important elements of a design for both a delay and energy point of view. In many electronics design low power consumption is basic need in most of the applications. The energy performance requirements enhance the most designers of next generation system towards the least possible power consumption. The power consumption is basically reduced by scaling of a power supply voltage. Flip flops typically consumes more than 50% of random logic power in the SoC chip, because of redundant transition of internal node.

Keywords: Flip-Flops, Low power, high-speed applications.

Introduction

Flip-flops (FFs) are the basic data storage elements used extensively in all kinds of digital designs. Particularly, digital designs nowadays often use intensive pipelining techniques and built many FF-rich modules such as register file, shift register, and first in first out. Traditionally, the demand for high performance was accessed by increasing clock frequencies with the help of technology scaling. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is nearly 50% of the total system power. FFs, thus, consumes a significant portion of the chip area and power consumption to the overall system design. Pulse-triggered FF (P-FF), having a single-latch structure, is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. Along with its speed advantage and simple circuitry P-FF helps to minimize the power consumption of the clock tree system.

A Pulse triggered flip-flop consists of a pulse generator for generating strobe signals and a latch for data storage. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. To obtain the balanced performance among power, area and delay, design space exploration is also a widely used technique.

In design practices, one pulse generation circuitry can be shared among FFs within the same register in explicit pulse generation. This gives the explicit type designs advantages in both circuit complexity and power consumption. In this paper, we will therefore focus on the explicit type designs only.To provide a comparison, some existing P-FF designs are reviewed rst. Fig. (a) Shows a classic

explicit P-FF design, named data-close to-output.

It contains a NAND-logic-based pulse generator and a semi dynamic true-single-phase-clock (TSPC) structured latch design. In this P-FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node X. The pulse width is determined by the delay of three inverters.

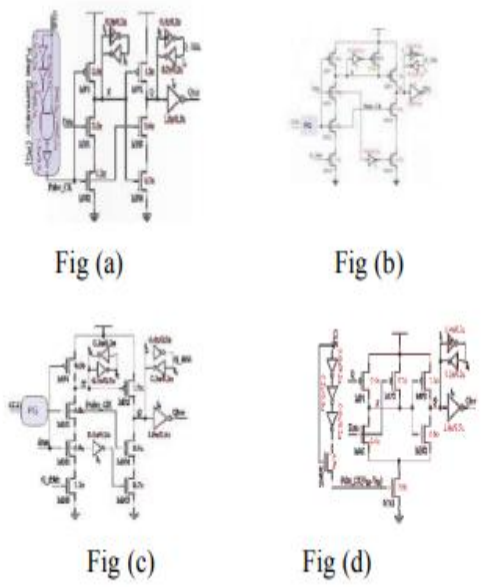

Figure 1: (a) ep-DCO (b) CDFF (c) Static CDFF (d) MHLFF

To overcome this problem, many remedial measures such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed. Fig. (b) shows a conditional discharged (CD) technique. An extra nMOS transistor MN3 controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains "1." In addition, the keeper logic for the internal node X is simpli ed and consists of an inverter plus a pull-up pMOS transistor only. The clock-gating in the conditional capture technique results in redundant power consumed by the gate controlling the de- livery of the delayed clock to the flip-flop.

Conditional discharge flip-flop

The flip-flop architecture into two categories i.e. conditional pre-charge and conditional capture technologies. This classification is based on how to prevent or reduces the redundant internal switching activities. Fig. 2 shows the conditional discharge technique, is proposed for both implicit type and explicit type pulse-triggered flipflops without the problems associated with the conditional capture technique. In this technique, the extra switching activity is reduced by controlling the discharging path when the input is stable HIGH and, therefore, the name given Conditional Discharge Technique. Therefore the conditional discharge is introduced to eliminate the switching activity at the internal nodes of flip flop.

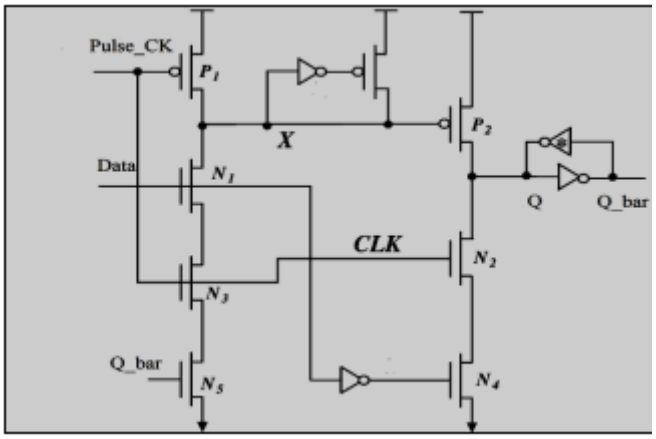

Figure 2: Conditional Discharge-Flip-Flop

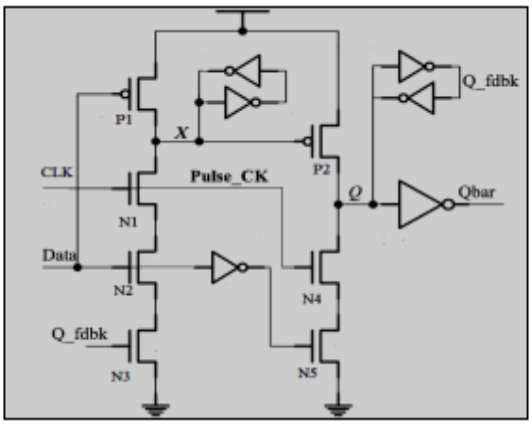

Figure 3: Static Conditional Discharged Flip - flop

Fig.3. shows the Static conditional discharge Flip-flop design. This structure differs from the CDFF design by using the static latch structure. So, the node X is not needed to be precharged periodically. This design exhibits longer D-to-Q delay than CDFF technique. Both the techniques face a worst case delay. This can be overcome by powerful pull down circuitry which consumes more power.

Conventional Explicit Type P-FF Design

PF-FFs, in terms of pulse generation, can be classified as an implicit or an explicit type. In an implicit type PFF, the pulse generator is part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse generator and the latch are separate. Without generating pulse signals explicitly, implicit type P-FFs is in general more power-economical. However, they suffer from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage. Its power consumption and the circuit complexity can be effectively reduced if one pulse generator is shares a group of FFs (e.g., an n-bit register). In this brief, we will thus focus on the explicit type P-FF designs only. To provide a comparison, some existing P-FF designs are reviewed first.

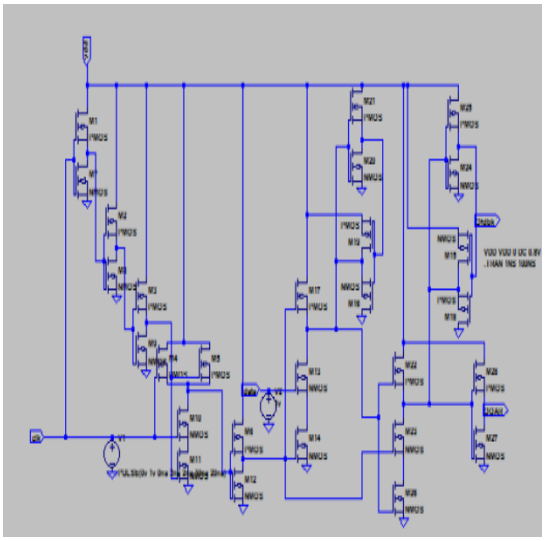

Figure 4: Conventional Explicit Type P-FF Designs

STATIC-CDFF

Above figure shows a similar P-FF design (SCDFF) using a static conditional discharge technique. It differs from the CDFF design in using a static latch structure. Node X is thus exempted from periodical recharges. It exhibits a longer data-to-Q (D-to-Q) delay than the CDFF design. Both designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption.

RESEARCH DESIGN

Recalling the four circuits reviewed in Section II, they all encounter the same worst case timing occurring at 0 to 1 data transitions. Referring to Fig. 5, the proposed design adopts a signal feed-through technique to improve this delay. Similar to the SCDFF design, the proposed design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. First, a weak pull-up pMOS transistor MP1with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design ,and the charge keeper circuit for the internal node X can be saved .In addition to the circuit simplicity, this approach also reduces the load capacitance of node X. Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme).Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed.

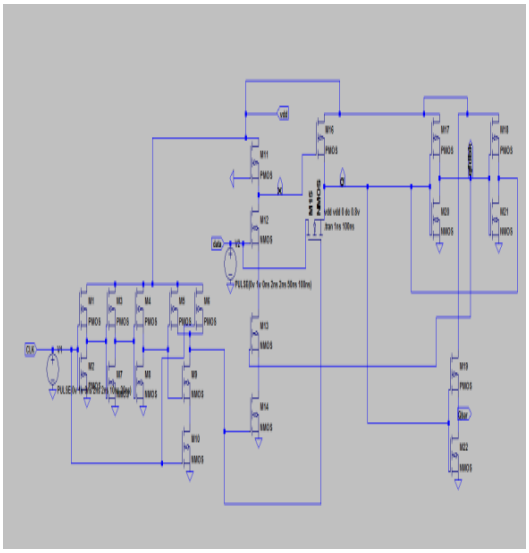

Figure 5: Schematic of Proposed Pulse-Triggered Flip-Flop

COMPARISON OF VARIOUS FF DESIGNS

Performance of FF Designs design does not use the least number of transistors; it has the smallest layout area. This is mainly attributed to the signal feed-through scheme, which largely reduces the transistor sizes on the discharging path. In terms of power behavior, the proposed design is the most efficient in five out of the six test patterns. The savings vary in different combinations of test pattern and FF design. For example, if a 25% data switching test pattern is used, the proposed design is more power economical than all except the ACFF design. Its power saving against ep-DCO, CDFF, SCDFF and MHLFF are 22.7%, 6.9%, 8.1% and 8.3% respectively. The ep-DCO design consumes the largest power because of the superfluous internal node discharging problem. ACFF design power efficiency is even more significant in the cases of zero or low input data switching activity.

SIMULATION RESULTS

The performance of the proposed P-FF design is evaluated against existing designs through post-layout simulations. A conventional CMOS NAND-logic-based

pulse generator design with a three-stage inverter chain is used for all P-FF designs except the MHLFF design, which employs its own pulse generation circuitry. The target technology is the TSMC 90-nm CMOS process. Since pulse width design is crucial to the correctness of data capture as well as the power consumption, the transistors of the pulse generator logic are sized for a design spec of 120 ps in pulse width in the TT case.

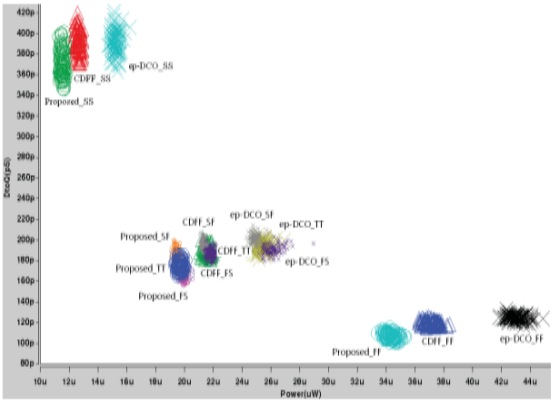

Figure 6: Monte Carlo simulation results

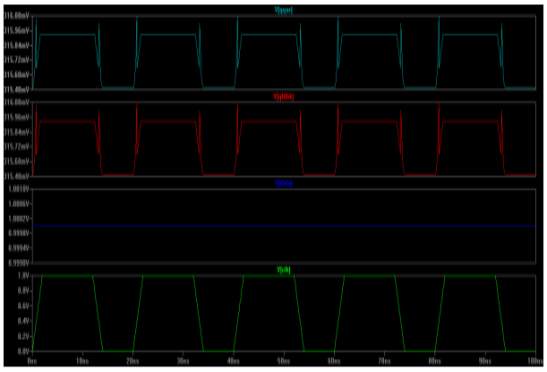

Figure 7: EP-FF simulation results

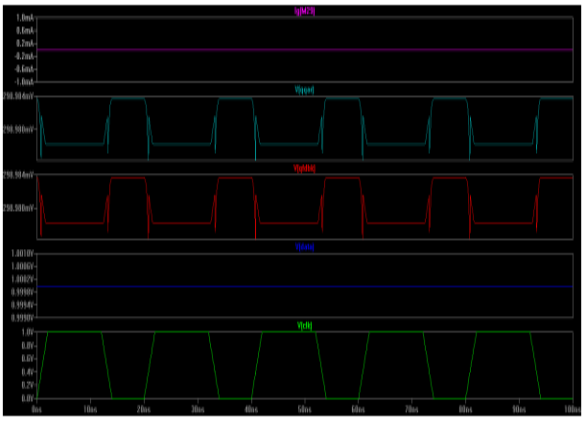

Figure 8: Static-CDFF simulation results

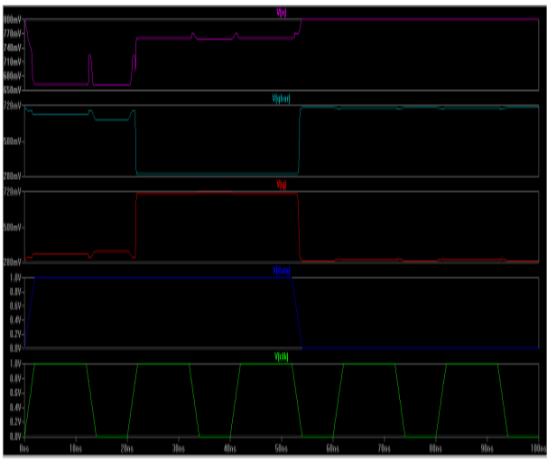

Figure 9: Proposed PFF Design Simulation Results

CONCLUSION

In this paper, the comparisons of various low power pulse triggered flip design is analyzed with several parameters like power, Layout, transistor count and delay. The Explicit Pulse Double Edge triggered Flip Flop (ep-DETFF) has limitations of high transistor count and occupies large area. The ep-DETFF has 2.27µW power differences when comparing it with Adaptive Coupling Configured Flip Flop. Supply voltage is mainly dependent on low power dissipation in future p-FF design by employing a modified latch structure. The design was intelligently achieved by employing a simple pass transistor. Extensive simulations were conducted, and the results did support the claims of the proposed design in various performance aspects.

References

1. *Gowri (2015) Design of Explicit Pulse Triggered Flip-Flop for Low Power Applications, International Journal of Advanced Information Science and Technology, ISSN: 2319:2682, Vol.4, No.3, DOI:10.15693/ijaist/2015.v4i3.158-162.*
2. *P S Keerthana (2016) TSMC-CMOS TECHNOLOGY BASED HIGH SPEED LOW POWER PULSE TRIGGERED FLIP*

FLOP, IJRSE, ISSN NO: 2319-8354, Vol. 5, Issue no: 1.

3. *Amruta S et al (2016) Low Power Explicit Pulse Triggered Flip-Flop Design Based On A Pass Transistor, International Journal of Advanced Engineering Research and Science, ISSN: 2456-1908, Vol-3, Issue-11.*
4. *F. Klass, C. Amir, A. Das, K. Aingaran, C. Truong, R. Wang, A. Mehta, R. Heald, and G. Yee, (1999) "A new family of semi-dynamic and dynamic flip-flops with embedded logic for high-performance processors," IEEE J. Solid-State Circuits, vol. 34, no. 5, pp. 712–716.*
5. *Jin-Fa (2013) Lin,Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-ThroughScheme"IEEE Trans, Very Large Scale Integr. (VLSI) Syst., 1063–8210/$31.00.*
6. *Xue-Xiang Wu and Ji-Zhong Shen, (2012)"Low-power explicit-pulsed triggered flip–flop with robust output," Electronics letter, Vol. 48 No. 24.*
7. *Peiyi Zhao et al (2004) High-Performance and Low-Power Conditional Discharge Flip-Flop, IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 12, No. 5.*
8. *M. Alioto, E. Consoli, and G. Palumbo (2010) General strategies to design nanometer flip-flops in the energy-delay space, IEEE Trans. CircuitsSyst., vol. 57, no. 7, pp. 1583– 1596.*