QUANTUM-DOT CELLULAR AUTOMATA BASED DESIGN OF FIVE INPUT MAJORITY GATE FULL COMMEMORATOR

Mrs.Sandhya Bolla,
Associate Professor
Department of ECE, Sri Indu College of Engineering & Technology, Hyderabad
sandy440@gmail.com

Ms. Deepika Rathod Bhukya
Associate Professor
Department of ECE, Sri Indu College of Engineering & Technology, Hyderabad.

Mrs. Prathyusha V
Associate Professor
Department of ECE, Sri Indu College of Engineering & Technology, Hyderabad.

Abstract:

In this paper, a novel quantum-dot cellular automata (QCA) comparator design is presented that reduces the number of QCA cells compared to previously reported designs. QCA is one of the few alternative computing platform that has the potential to be a promising technology because of higher speed, smaller size, and low power consumption in comparison with CMOS technology. The proposed design is compared with previous works in terms of complexity, area. In comparison with the best previous full comparator, our design has improvement in cell count and area. This paper also presents a modified MAJ_5 gate with a greater fault tolerance.

Keywords—Quantum-dot Cellular Automata, QCA Cell, MAJ_5

INTRODUCTION

Over the years, engineers have been able to continuously shrink the size of CMOS transistors and thereby package more of them on the same chip. However as we approach the physical limits of photo-lithography as well as device physics, this task has become more expensive and complicated. Studies show that the progress towards increasing chip complexity while maintaining the speed and constructing the power dissipation has slowed considerably. It is now believed that within the next two decades, the semiconductor industry will have to start using new nanoelectronic devices [1] .The international roadmap for semiconductors has enumerated several nanoelectronics alternatives including Resonant tunneling diodes (RTD), QCA, Tunneling Phase Logic (TPL)[2].Amongst all these technologies , QCA promises to provide the highest device density with low power consumption and high switching speeds[3]. In addition QCA uses the same technology to build both, the logic gates and the wires carrying logic signals. Even though QCA has attractive properties, building large QCA architectures has not been very successful.

The primary limitation to QCA is the availability of only two basic building blocks: an inverter and a three input majority gate (MAJ3) shown in Fig.1 .Though the MAJ3 gate can be configured as a two input AND or OR gate , building larger architecture with two input gates is laborious. Such architecture tends to have high complexity, difficult connectivity and low reliability. This paper introduces a new powerful building for QCA technology, a five input majority gate. We also provide a most robust version of MAJ5 gate which functions correctly in more than 40% of the cases of missing a single QCA Cell in the structure.

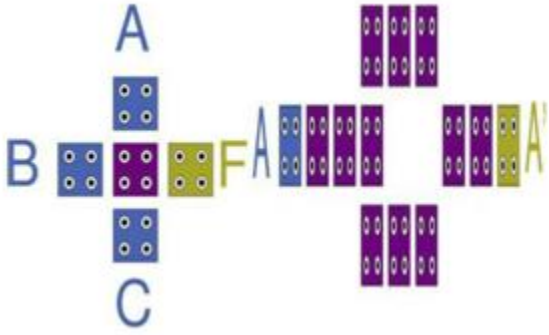

Fig 1:The only gates in QCA technology : a three input majority gate (left) and inverter.

QCA BASICS

The fundamental unit of QCA is QCA cell, which is composed of four quantum dots , as shown in fig 2(a).The cell is charged with two extra electrons , which tend to occupy diagonally opposed dots as a result of their coulomb repulsion . The electrons are permitted to jump between the various quantum dots in a cell by mechanism of quantum mechanical tunneling, but they are not permitted to tunnel between the two individual cells [2].Thus , there are two possible arrangements denoted as cell polarization P=+1 and P=-1.By using cell polarization P=+1 represents logic 1 and P=-1 represents logic 0, binary information can be encoded . Arrays of QCA cells can be arranged to perform wire and all logic functions[3].Instead of the traditional metal wire ,the QCA wire is used to construct a digital logic ciucuit.In a QCA wire, the binary signal propagates from input to output because of the electrostatic interactions between the cells. There are two kind of QCA wires as shown in Fig 2(b) and Fig 2(c).One is a binary wire implemented with cells of 90º orientation, and the other is an inversion chain implemented with the cells of 45º orientation.

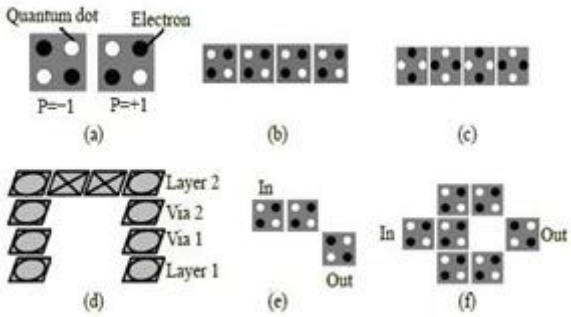

Fig 2: (a)QCA cell (b)binary wire (c)QCA inversion chain (d)QCA Multilayer crossing (e) inverter type1 (f) inverter type 2

OA> B = A. B

OA< B = A.B

OA= B = OA> B .OA< B

Eqn 1

Also, the equations for full comparator are given by

OA> B = A. B .C

OA< B = A.B.C

OA= B = OA> B .OA< B

Eqn 2

Any QCA circuit can be efficiently built using only majority gates and inverters. The simplest structure of the inverter, shown in Fig2(e) , is usually formed by placing the cells only with their corners touching. In Fig2 (f) the 45º displacement in the two lines of merging cells produces the complement of the input signal.

Where for an n-bit full comparator, the output OA=B of one stage is fed directly to the input C of the next stage . The logic diagram of a full comparator is presented

in Fig 4(a). Equations of a full comparator realized with majority gates and inverters are shown below:

A FIVE INPUT MAJORITY GATE

A five input majority gate MAJ5, is a Boolean gate whose

$OA> B = M(M(A, B, -1), -1, C)$,

output is 1only if 3 or more of its input are 1.The Boolean expression of MAJ_5 is given by :

MAJ_5 (A, B, C, D, E) = ABC + ABD + ABE + ACD+ACE + ADE + BCD + BCE + BDE + CDE

The proposed implementation of the MAJ_5 gate is shown in Fig 3.

The MAJ_5 gate was simulated using the QCA Designer version 2.0.3 [7]in all simulations given in this paper , we used the coherence vector computational engine and the following parameters: 10nmX10nm cell size, 2.5nm cell-cell distance , 2.5nm dot size and 40nm radius of influence this are the parameters employed by [4] –[6].

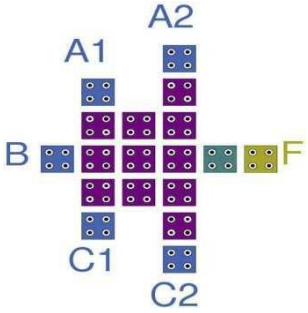

Fig 3: A five input majority gate

DESIGN APPROACH

Comparator is one of the important components in logic design. Comparators are used in central processing units (CPUs) and microcontrollers. If we assume that the inputs are A and B and the outputs are OA=B, OA>B and OA<B, the logical functions of the half comparator can be expressed as *A= B* *A>B* *A<*B

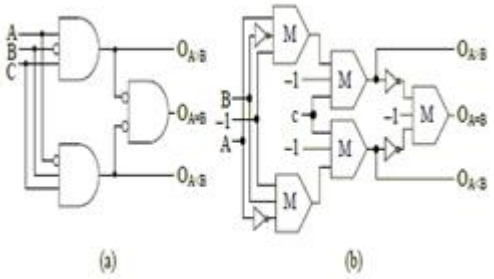

Fig 4:(a)logic diagram (b)schematic diagram

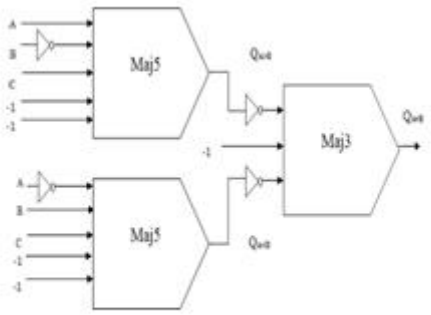

Fig 4(c): Full comparator using majority gates

RESULTS AND DISCUSSION

The QCA implementation of the proposed full comparator is simulated by the QCA Designer tool [8]. The following parameters are used for a bistable approximation : cell size=18 nm×18 nm, number of samples=12,800, radius of effect=65 nm, relative permittivity=12.9, convergence tolerance=0.0001, clock high=9.8e-22J, clock low=3.8e-23J, clock amplitude factor=2, layer separation=11.5 nm and maximum iterations per sample=100. Also, the diameter of the quantum dot is 5 nm and the cell distance is 2 nm.. Table 1 show the comparison between the proposed full comparator and the previous ones. As shown in Table 1, full comparator has resulted in significant improvements in terms of area, complexity. In comparison with the best previous full comparator design presented in [9], the proposed full comparator has 85% improvement in the area, 64% improvement in cell count, and 95% improvement in the wasted area in the cells. In comparison with the best previous

half comparator presented in [10], our design has 62% improvement in the area 16% improvement in the cell count,and 90% improvement in the wasted area in cells. Also, our comparator is faster than the previous ones. From these results, it is evident that the proposed full comparator is improved as compared to the previous ones.

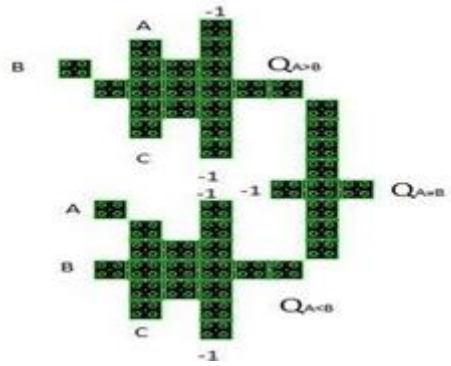

Fig5: Layout of 5 Input majority gate full Comparator Table1: Comparison of QCA Comparators

CONCLUSION

In this paper, a novel scheme for QCA cell has been introduced to construct a five input majority gate in order to make efficient QCA majority logic design. As a case study , the proposed technique is used to develop a full comparator that is constructed with two MAJ5 , one MAJ3 and four inverters. The QCA full comparator has been compared with the previous best comparator so far designed. It is expected that the new scheme for QCA cells and the new form of majority gate and the reduction method presented in his paper produces significant improvement in majority gate based nanoelectronic circuits and reduces chip area and increases speed for many future QCA architectures.

REFERENCES

[1]. D. A. Antonelli, D. Z. Chen, T. J. Dysart, and X. S Hu, "Quantum- dot cellular automata (QCA) circuit partitioning: Problem modeling and solutions," in Proc. of Design Auto. Conf., (San Diego,CA), June 2004.

[2]. M.T. Niemir, Designing Digital Systems in Quantum Cellular Automata, MSc Thesis, Department of Computer Science and Engineering Notre Dame, Indiana, 2004.

[3]. K. Walus, V.S. Dimitrov, and G.A. Julliaen, "Computer Architecture Structure for Quantum Cellular Automata,"3rdIEEE Nanotech. Conf., 2003, p. 1435.

[4]. J. Huang, M. Momenzadeh, L. Schiano, M. Ottavi, and F. Lombardi, "Tile-based QCA design using majority-like logic primitives," ACM J. on Emerging Technologies in Computing Systems, vol. 1, pp. 163-185, October 2005.

[5]. M. Momenzadeh, M. Ottavi, and F. Lombardi, "Modeling QCA defects at molecular-level in combinational circuits," IEEE Trans. on Nanotechnology, pp. 208-216, October 2005.

[6]. J. Huang, M. Momenzadeh, and F. Lombardi, "On the tolerance to manufacturing defects in molecular QCA tiles for processing-by-wire," J. of Electronic Testing: Theory and Applications, vol. 23, pp. 163-174, June 2007.

[7]. K. Walus, T. J. Dysart, G. A. Jullien, and A. R. Budiman, "QCADesigner: A rapid design and simulation tool for quantum-dot cellular automata," in IEEE Trans.Nanotechnology, 2004.

[8]. "QCADesigner," The University of British Columbia,2011.http://www.mina.ubc.ca/qcadesigner

[9]. Y. Xia and K. Qiu, "Design and Application of Universal Logic Gate Based on Quantum-Dot Cellular Automata," 11th IEEE Intern. Conf. Comm. Tech. Proc., 2008, p. 335.

[10]. Y.-S. Xia and K.-M. Qiu, "Comparator Design Based on Quantum-Dot Cellular Automata," J. Electron. Info. Technol., vol.31, no. 6, 2009, pp. 1517-1520.

	Previous Work	Proposed work
Level	3	2
Inverter	4	4
Majority Gates	5 MAJ3	2 MAJ5,1MAJ 3

Author's Profile:

1)Mrs. Sandhya Bolla is currently working as Associate Professor, Department of ECE in Sri Indu College of Engineering & Technology, Hyderabad. She received the B.Tech. Degree in Electronics and Communication Engineering and the M.Tech. Degree in Embedded Systems from JNTU

Hyderabad. She has got 12 years of teaching experience. She has 11 research publications. Her research interests include digital communications, signal processing, wireless, cellular and mobile communications, and Massive MIMO techniques.

2)Ms. Deepika Rathod Bhukya is currently working as Associate Professor, Department of ECE in Sri Indu College of Engineering & Technology, Hyderabad. She received the B.Tech. Degree in Electronics and Communication Engineering and the M.Tech. Degree in Digital Electronics and Communication Systems from JNTU Hyderabad (JNTUH), India. She has got 12 years of teaching experience. She has 5 research publications. Her research interests include Microwave and Radar Signal Processing, Digital Communications, Signal Processing, Wireless, Cellular and Mobile Communications, and Massive MIMO Techniques.

3)Mrs. Prathyusha V is currently working as Associate Professor, Department of ECE in Sri Indu College of Engineering & Technology, Hyderabad. She received the B.Tech. Degree in Electronics and Communication Engineering and the M.Tech. Degree in Embedded Systems from JNTU Hyderabad (JNTUH), India. She is currently pursuing the Ph.D. Degree with the Department of Electronics and Communication Engineering, Osmania University, Hyderabad, Telangana. she has got 14 years of teaching experience. She has 12 research publications. Her research interests include Digital Communications, Signal Processing, Wireless, Cellular and Mobile Communications, and Massive MIMO Techniques.