IMPLIMENTATION OF LOW POWER SHIFT REGISTER USING PULSED LATCHES

BANDI MYTHILY DEVI
Reg No: 26616130
Research Scholar
Dept of ECE
SHRI JJT UNIVERSITY
RAJASTHAN

Dr. Kasa Chiranjeevi
JJT/2K9/ENG/681
Assistant Professor,
Electrical and Electronics Engineering,
SHRI JJT UNIVERSITY
RAJASTHAN

Dr. Md. Uzma Afreen
JJT/2K9/ENGG/698
DEPARTMENT OF ECE
SHRI JJT UNIVERSITY
RAJASTHAN

ABSTRACT
Shift register is the key element to translate the parallel data to serial form or vice versa in digital circuits. It is commonly used in many applications, such as digital filters communication receivers, and image processing ASIC's. It can also a function as delay circuits and digital pulse extenders. In the existing system, the conventional N-bit unidirectional shift-register was proposed and it consists of N number of master-slave flip-flop with multiple 2-to-1 multiplexers. Also, the conventional clock signal methodology was promoted to transfer data from one stage to next stage. It occupies more silicon area and increases the power consumption of the shift register. To eradicate the above said difficulties a novel 256-bit bidirectional shift-register using BD-PLs is proposed. It simplifies the BD-PL structure by removing the contemporary signals (Qb, DR_b, and, DL_b) and also reduce the number of full swing clock signals applied to each stage. The modified method will reduce area and power consumption of the bidirectional shift register. The proposed method will be implemented using the XILINX Software technology.

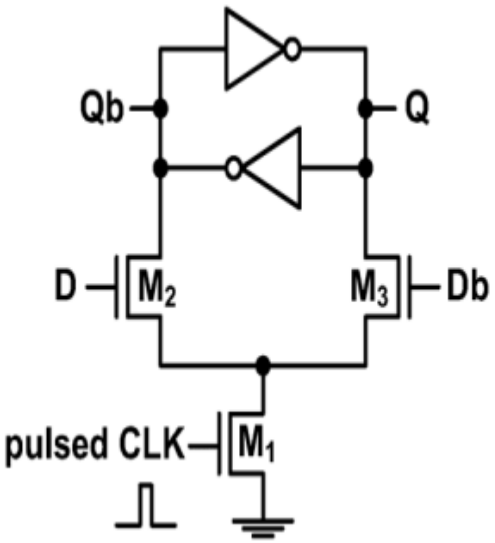
Keywords: *Area-efficient, bidirectional shift-register, flip-flop, pulsed clock, pulsed-latch.*

Introduction
A shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers, and image processing ICs. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register. A 16-megapixel CMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. The architecture of a shift the shift registers.

ARCHITECTURE
A. SHIFT REGISTER:
The Existing method comprises of the design of the shift register by using pulsed latches. Moreover the Architecture of the shift register consists of pulsed clock generator which is used for generating clock pulses to the latches. Then, it also consists of sub-shift registers blocks and it also contains temporary storage latch to produce some time delay.

B. Ssaspl latch
As shown in the figure(1)static differential sense amp shared pulse latch).It consists of 7 transistors. The latch consists of one cross coupled inverters and it also consists of 3 NMOS transistors (M1-M3). The lowest clock power has been achieved because the pulsed clock signal is shared with one single transistor M1.Thecomplementary data ouput has been obtained based on the data input D

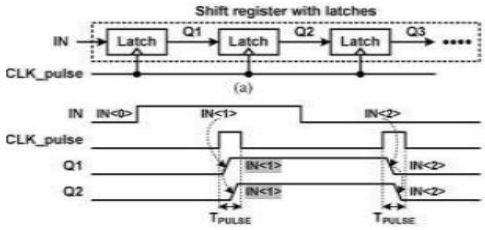
and Db. The three NMOS transistors has been designed as such transistors has been used to hold the data with four transistors (cross-coupled-inverters). It also needs differential data inputs and pulsed clock signal. If the pulsed clock signal input is high so it updates the data. The node q or qb is pulled down to ground according to the complementary data inputs. The output signals of the first latch (Q1 and Q1b) change correctly, because the input signal of the first latch (IN) is constant during the clock pulse width .On the other hand, the output signals of the second latch (Q2 and Q2b) do not change, because the input signals of the second latch, which are connected to the output signals of the second latch (Q2 and Q2b), change during the clock pulse width. The SSASPL flip the states of the cross-coupled inverters (Q and Qb) by pulling current down through either or during the clock pulse width. The clock pulse width is selected as the minimum time to flip the output signals of the latch (Q and Qb) when its input signals (D and Db) are constant. If the input signals change during the clock pulse width, the time pulling current down through either or becomes shorter than the clock pulse width, so that the latch has not enough clock pulse time to flip the output signals after the input signals change.



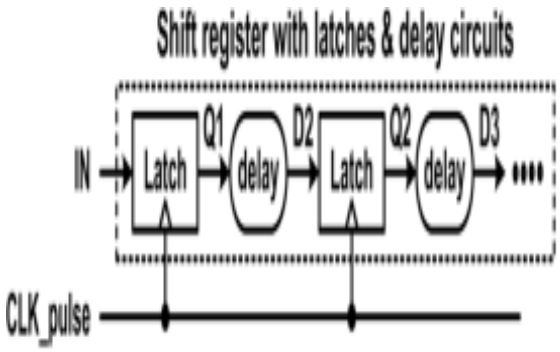
Schematic of the SSASPL

PROPOSED METHOD

Generally Shift Register Can Be Implemented ByUsing The Latch Is shown in the below Figure2. In that if we apply clock signal to that shift register which is encompassed of latches the individual latch outputs delayed by one bit because of single clock pulse is used to produce the outputs shown in the figure

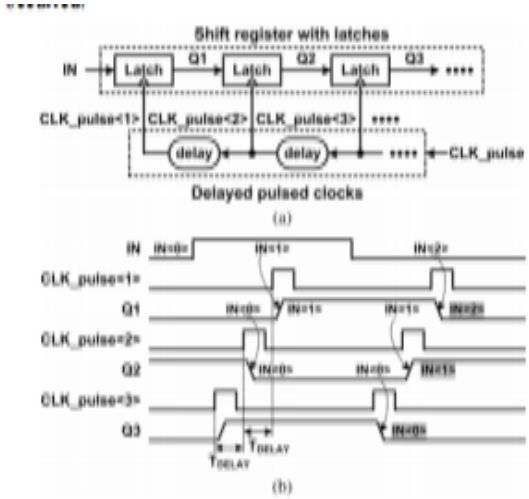


To avoid delay in the circuits two possible methods are there one is adding the delay elements in between the latches delay element is inserted it can compensate the delay associated by the clock propagation so that timing problem can be overcome it is shown in the Figure 3 another method is using non overlapping clock method delay can be avoided

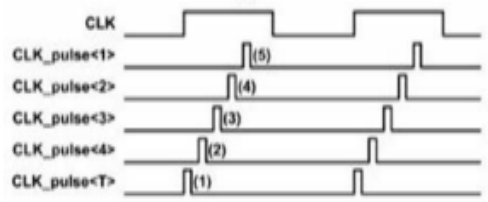


Implementation of Shift Register by using the delay lines

In this method every latch pulsed using clock signal and to reduce the un certainty in the out put of next latch delay element is inserted. Hence every latch updates the new value during its clock period itself only then no timing problems is occurred.



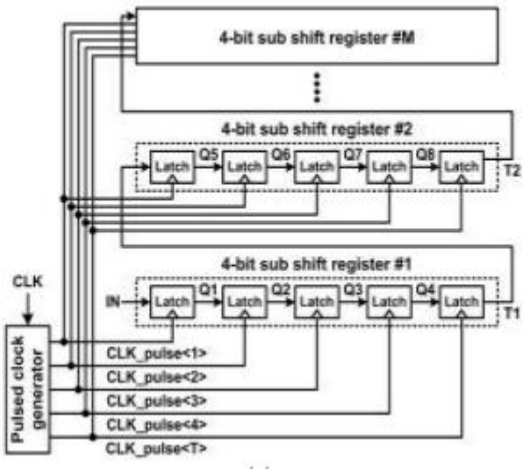
Proposed circulate check in: An ace slave turn-flop is synthetic the usage of hook in fig. 1 (a) may be supplanted with a beat hook that has a lock and a beat test sign as in Fig. 1 (b). All hook uses heartbeat clock generator circuit for beat clock signal. therefore, the proposed move register vicinity and beat lock energy decreases sort of 50% of the turn-flops. Beat hook alternate is an attractive answer for low field and coffee power programs. The beat lock cannot be utilized legitimately in circulate enlists because of the time types of clock signal,The circulate join up incorporates of sure hooks and a beat clock signal (CLK_pulse). The yield signal of the primary lock refreshes successfully in view that the information sources signal of the primary hook (IN) is everyday within the path of the clock beat width. Be that as it is able to, the following hook has a doubtful yield sign (Q2) due to the fact its facts sign (Q1) modifications at some point of the clock beat width. One solution for the making plans kinds is to encompass deferred circuits among locks; The yield signal of the hook is postponed and arrives at the subsequent lock after the clock beat. The yield signal of the primary and second locks updates in the direction of the clock beat width, but the statistics signal of the second one and 0.33 hooks emerge as same to the yield sign of the primary and 2nd locks after the clock beat. Ultimately, all of the hook have consistent information indicators at a few stage in the clock beat and there can be no planning problem among the lock. Be that as it may, the put off circuit reasons giant location and power overhead. Any other association is to utilize numerous postponed beat clock indicators. The deferred beat clock sign are produced whilst a clock sign reviews delay circuits the numerous clock heartbeats will created. Each lock makes use of a beat clock signal that is deferred with the aid of way of the beat check sign applied in its next hook. In the end, every lock adjustments the information when its subsequent hook refreshes the statistics. Subsequent to associating the put off circuit each hook has a comparable contribution throughout the clock beat and there may be no time variety between the lock. Be that as it is able to, this association likewise calls for numerous get rid of circuits.



Diverse postponed beat clock indicators

Shift register with latches, delay circuits, and a pulsed clock signal. (a)Schematic (b)Waveforms.

bitsub shifter register comprising of five latches and it presents shift operations with five non overlap delayed pulsed clock signals (CLK_pulseand CLK_pulse). In the 4-bit sub shift register #1, four latches store 4- bit data (Q1-Q4) and the last latch saves 1-bit temporary data (T1) which will be saved inthe first latch (Q5) of the 4-bit sub shift register #2. Fig. 4(b)shows the operation waveforms in the proposed shift register. The amount of latches and clockpulse circuits vary according to the word length of the sub shift register is selected by considering the space, power dissipation, speed.



Proposed shift register(a)Schematic (b)Waveforms.

Area Optimization:

The area optimization can be performed as follows. When the circuit areas are normalized with a latch, the areas of a latch and a clock pulse circuit are 1 and 0,respectively.The total area becomes + + + × A α((K 1) N(1 1/ K) The optimal K= AαN / for the minimum area is obtained from the first order differential equation of the total area. An integer for the minimum area is selected as a divisor of which is nearest to AαN / Power Optimization: The power optimization is similar to the space optimization. The power is disbursed mainly in latches and clock-pulse circuits. Each latch paid out power for data transition and clock loading. When the circuit powers are regularized with a latch, the power dissipation of a latch and a clock-pulse circuit are 1 and 0 correspondingly. The total power dissipation is also .An integer for the minimum power is preferred as a divisor of, which is closer to Chip Implementation: The highest clock frequency in the conventional shift register is confined to only the delay of flip-flops because there is no delay in the midst of flip-flops. Therefore, the space and power dissipation are more significant than the speed for choosing the flip-flop. The proposed shift register uses latches on behalf of flip-flops to decrease the area and power dissipation.

Conclusion

In this paper we have explained that the shift registers designed with the pulse triggered flip-flop is said to have low power consumption, low delay, the average power is less and the power delay product is also reduced when compared to the shift registers designed with normal flipflops. In this technique is reducing time consumption. This has been implemented in real time systems and has proved its properties. This paper proposed a low-power and areaefficient shift register using pulsed latches. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved

using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal. A 256- bit shift register was fabricated using a 0.18 micrometers CMOS process with VDD=1.8V.

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