# LOW POWER AND AREA – EFFICIENT SHIFT REGISTER WITH APPROACH OF PULSED LATCHES

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## ABSTRACT
*This paper proposes a low-power and area-efficient shift register using pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 128-bit shift register using pulsed latches was fabricated using a 65nm CMOS process with VDD = 1.0V. The proposed shift register saves area and power compared to the conventional shift register with flip-flops.*

***Keywords:*** *Area-efficient, flip-flop, pulsed clock, pulsed latch, shift register.*

## Introduction
A Shift Register is the basic building block in VLSI circuit Shift registers are commonly used in many applications, such as digital filters, communication receivers, and image processing ICs . The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications. This paper proposes a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

## PROPOSED SYSTEM
A master-slave flip-flop using two latches in Fig. 1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1(b)[6]. All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption. The pulsed latch cannot be used in shift registers due to the

timing problem, as shown in Fig. 2. The shift register in Fig. 2(a) consists of several latches and a pulsed clock signal (CLK_pulse). The operation waveforms in Fig. 2(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signal of the first latch (IN) is constant during the clock pulse width. But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 3(a). The output signal of the latch is delayed and reaches the next latch after the clock pulse. As shown in Fig. 3(b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock. Pulse and no timing problem occur between the latches. However, the delay circuits cause large area and power overheads. Another solution is to use multiple non-overlaps delayed pulsed clock signals, as shown in Fig. 4(a). The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits

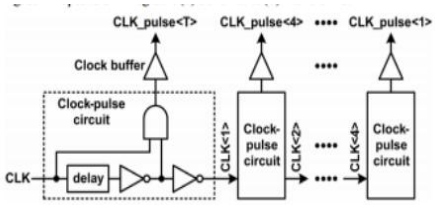


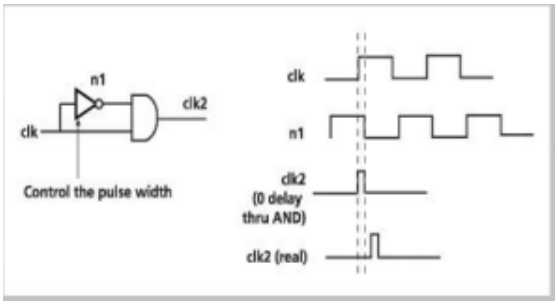

Figure 1. Delayed clock pulse register

The proposed shift register is divided into sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs and⟩1:4⟨shift operations with five non-overlap delayed pulsed clock signals (CLK_pulse ). In the 4-bit sub shift register #1, four latches store 4-bit data (Q1-Q4) and the⟩T⟨CLK_pulse last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4- bit sub shift register #2. Fig. 5(b) shows the operation waveforms in the proposed shift register. Five non-overlap delayed pulsed clock signals are generated by the delayed pulsed clock generator in Fig. 6. The sequence of the pulsed clock signals is in the opposite order of the five updates the latch data T1 from Q4. And⟩T⟨latches. Initially, the pulsed clock signal CLK pulse update the four latch data from Q4 to Q1⟩1:4⟨then, the pulsed clock signals CLKpulse sequentially. The latches Q2–Q4 receive data from their previous latches Q1–Q3 but the first latch Q1 receives data from the input of the shift register (IN). The operations of the other sub shift registers are the same as that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous sub shift register The proposed shift register reduces the number of delayed pulsed clock signals significantly, but it increases the number of latches because of the additional temporary storage latches. As shown in Fig. 6 each pulsed clock signal is generated in a clock-pulse circuit

consisting a delay circuit and an AND gate. When an shift register is divided into sub shift registers, the number of clock-pulse circuits is and the number of latches. A sub shift register consisting of latches requires pulsed clock signals. The number of sub shift registers becomes, each sub shift register has a temporary storage latch. Therefore, latches are added for the temporary storage latches. The conventional delayed pulsed clock circuits in Fig. 4 can be used to save the AND gates in the delayed pulsed clock generator in Fig. 6. In the conventional delayed pulsed clock circuits, the clock pulse width must be larger than the summation of the rising and falling times in all inverters in the delay circuits to keep the shape of the pulsed clock. However, in the delayed pulsed clock generator in Fig. 6 the clock pulsed width can be shorter than the summation of the rising and falling times because each sharp pulsed clock signal is generated from an AND gate and two delayed signals. Therefore, the delayed pulsed clock generator is suitable for short pulsed clock signals. The numbers of latches and clock-pulse circuits change according to the word length of the sub shift register. is selected by considering the area, power consumption, speed. In a long shift register, a short clock pulse cannot through a long wire due to parasitic capacitance and resistance. At the end of the wire, the clock pulse shape is degraded because the rising and falling times of the clock pulse increase due to the wire delay. A simple solution is to increase the clock pulse width for keeping the clock pulse shape. But this decreases the maximum clock frequency. Another solution is to insert clock buffers and clock trees to send the short clock pulse with a small wire delay. But this increases the area and power overhead. Moreover, the multiple clock pulses make the more overhead for multiple clock buffers and clock trees.

**PULSED LATCHES**

The pulsed latch requires pulse generators that generate pulse clock waveforms with a source clock. The pulse width is chosen such that it facilitates the transition. The following diagram represents a simple pulse generator and the associated pulse waveform. In this methodology, the pulse generators are automatically inserted to satisfy several rules during clock-tree synthesis. Along with pulse generators, this approach also uses a number of matching delay cells to allow
for match clock insertion delays with or without pulse generators.




**A. Shift registers**

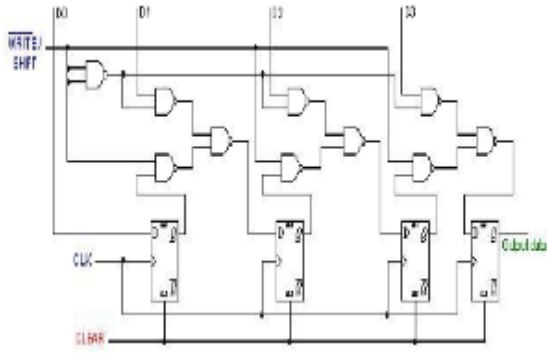
Flip flops are use in constructing registers. Register is a group of flip flops used to store multiple bits of data. For example, if a computer is to store 16 bit data, then it needs a set of 16 flip flops. The input and outputs of a register are may be serial or parallel based on the requirement. A shift register is a sequential circuit which stores the data and shifts it towards the output on every clock cycle. Basically shift registers are of 4 types. They are

- Serial In Serial Out shift register
- Serial In parallel Out shift register
- Parallel In Serial Out shift register
- Parallel In parallel Out shift register

**B. Parallel in Serial out shift register**

The input to this register is given in parallel i.e. data is given separately to each flip flop and the output is

collected in serial at the output of the end flip flop. The clock input is directly connected to all the flip flops but the input data is connected individually to each flip flop through a mux (multiplexer) at input of every flip flop. Here D1, D2, D3 and D4 are the individual parallel inputs to the shift register. In this register the output is collected in serial



Parallel in serial out shift register.

**Parallel In serial out Shift Register**

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In show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signal of the first latch (IN) is constant during the clock pulse width .But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width. One solution for the timing problem is to add delay circuits between latches. The output signal of the latch is delayed and reaches the next latch after the clock pulse. As shown in the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock.

**PULSED LATCH ARCHITECTURE**

The power optimization is similar to the area optimization. The power is consumed mainly in latches and clock-pulse circuits. Each latch consumes power for data transition and clock loading. When the circuit powers are normalized with a latch, the power consumption of a latch and the clock-pulse circuit are 1 and respectively.The total power consumption is also .An integer for the minimum power is selected as a divisor of, which is nearest to. In selection, the clock buffers are not considered. The total size of the clock buffers is determined by the total clock loading of latches. Although the number of latches increases from to, the increment ratio of the clock buffers is small. The number of clock buffers is , As increases, the size of a clock buffer decreases in proportion to because the number of latches connected to a clock buffer is proportional. Therefore, the total size of the clock buffers increases slightly with increasing and the effect of the clock buffers can be neglected for choosing. The maximum number of is limited to the target clock frequency.

As the minimum clock cycle time is , where is the delay from the rising edge of the main clock signal (CLK) to the rising edge of the first pulsed clock signal (CLKpulse(T)), is the delay of two

neighbour pulsed clock signals, is the delay from the rising edge of the last pulsed clock signal (CLKpulse(1)) to the output signal of the latch Q1 is proportional to . As increases, the maximum clock frequency decreases in proportion to. Therefore, must be selected under the maximum number which is determined by the maximum clock frequency of the target applications. The pulsed clock signals are supplied to all sub shift registers. Each pulsed clock signal arrives at the sub shift registers at different time due to the pulse skew in the wire. The pulse skew increases proportional to the wire distance from the delayed pulsed clock generator. All pulsed clock signals have almost the same pulse skews when they arrive at the same subshift register. Therefore, in the same sub shift register, the pulse skew differences between the pulsed clock signals are very small. The clock pulse intervals larger than the pulse skew differences cancel out the effects of the pulse skew differences. Also, the pulse skew differences between the different sub shift registers do not cause any timing problem because two latches connecting two sub shift registers use the first and last pulsed clocks(CLK_pulse(T)and CLK_pulse(1)) which have a long clock pulse interval.

## CONCLUSIONS

This paper proposed a low power and area efficient shift register using pulsed latches the shift register reduces area and power consumption by substituting flip flop with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals as an alternative of a single pulsed clock signal. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal. A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 256-bit shift register was fabricated. The proposed shift register saves 37% area and 44% power compared to the conventional shift register with flipflops.

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