IMPLEMENTATION OF SVPWM TECHNIQUE TO VOLTAGE AND CURRENT SOURCE INVERTER

Dr. M.Rajendar Reddy Professor& Head, Dept. of EEE,

Mahaveer Institute of Science & Technology, Hyderabad, India. Rajendar1956@gmail.com

Abstract—The importance of this paper is implementation and control of the converters using space vector pulse width modulation (SVPWM) technique to VSI and CSI converters. The SVPWM pulses are given to converter and analyze the THD at different switching frequencies and comparing them on modulation index. This paper focuses on step-by-step development of SVPWM model and comparing them on various parameters. The three phase VSI and CSI models are discussed based on space vector theory. The simulation results are obtained for effectiveness of study

Keywords—VSI, CSI, SVPWM,THD,Modulation Index.

I. INTRODUCTION

Converters can be classified as rectifiers (AC-to-DC converter), inverters (DC-to- AC converter), choppers (DC- to-DC converter), AC power controller (at same frequency), and cyclo-converter (direct frequency changer).

Research has been going on different modulation strategies to modulate these converters for an efficient use. Many techniques have been proposed in order to have a minimum amount of switching in the converter and also to synthesize output voltages and output currents with very high gains. The SVPWM is considered as an enhanced technique for PWM implementation because it is having some of the advantages over SPWM in terms of good utilization of DC bus voltage, reduced switching frequency and low current ripple. SVPWM provides succeeding the advantages:

i) Better fundamental output voltage

G.Premkumar Reddy

Associate Professor, Dept. of EEE, Mahaveer Institute of Science & Technology, Hyderabad, India. Gpkreddy2009@gmail.com

- ii) Better Harmonic performance and THD
- iii) Easier hardware implementation in digital signal processor [1], [6].

In this paper, SVPWM scheme is proposed for three- phase inverters. This modulation scheme is very useful in the modulation of VSI and CSI. This paper focuses on step-by-step development SVPWM Model, applying it to VSI and CSI and comparing them on various parameters i.e., for different switching frequency, different load parameters and same modulation index. The model of a three-phase VSI and CSI are discussed based on space vector (SV) theory [8], [9].

BLOCK DIAGRAM



Fig.1 Block diagram of the proposed system

The overall block diagram for the proposed system is shown in Fig.1.The Principle of SVPWM

- Treats the sinusoidal voltage as a constant amplitude vector rotating at constant frequency.
- The PWM technique approximates the reference voltage Vs by a combination of 8 switching pattern.

Steps followed in realization of SVPWM is as under

• Determining Va, Vb, Vref and reference angle θ .



- Determining time duration T1, T2and T0.
- Determining the switching time of each switch.
 - II. SPACE VECTOR PULSE WIDTH MODULATION

A. SVPWM for Voltage Source Inverter

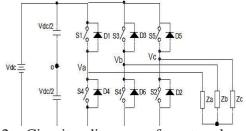
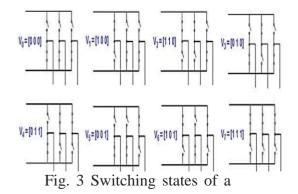


Fig.2 Circuit diagram for two-level Voltage Source Inverter

The Fig.2 shows two-level VSI. It is having 6 switches (S1 to S6) and each of these switches is represented with MOSFET/IGBT depending upon the type of power application. The major difference of SVPWM with other PWM techniques is that, it uses vector as reference [2].

The Inverter leg switching states are represented in Fig.3 If the upper switches 1, 3 and 5 are one, then the switch is ON

If the upper switches are zero then the terminal voltages are zero. The only possible combinations of the switching states: 000, 001, 010, 011, 100, 110, 101, and 111 which are shown in Fig. 3[2].



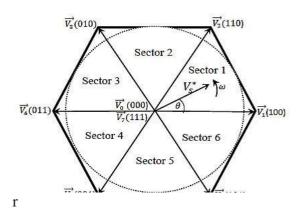
Voltage source inverter

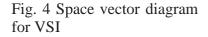
The ON and OFF states transistors can be used to determine the output voltage which is given in the Table 1.

Table 1Space vectors, switching states and on-State Switches

| Space vector | | Switching States | On-state Switch | Vector definition |
|--------------|-------------|---------------------|--------------------|---------------------------------------------------------|
| Null vector | \vec{V}_7 | [1 1 1] | S_1, S_3, S_5 | 0 |
| | \vec{V}_0 | [0 0 0] | S_4, S_6, S_2 | 0 |
| | \vec{V}_1 | [1 0 0] | S_1, S_6, S_2 | $\vec{V}_1 = \frac{2}{3} V_{dc} * e^{j0}$ |
| | \vec{V}_2 | [1 1 0] | S_1, S_3, S_2 | $\vec{V}_2 = \frac{2}{3} V_{dc} * e^{j\frac{\pi}{3}}$ |
| Active | \vec{V}_3 | [0 1 0] | S_4, S_3, S_2 | $\vec{V}_3 = \frac{2}{3} V_{dc} * e^{j\frac{2\pi}{3}}$ |
| vector | \vec{V}_4 | [0 1 1] | S_4, S_3, S_5 | $\vec{V}_4 = \frac{2}{3} V_{dc} * e^{j\frac{3\pi}{3}}$ |
| | \vec{V}_5 | [0 0 1] | S_4, S_6, S_5 | $\vec{V}_5 = \frac{2}{3} V_{dc} * e^{j\frac{4\pi}{3}}$ |
| | \vec{V}_6 | [1 0 1] | S_1, S_6, S_5 | $\vec{V}_6 = \frac{2}{3} V_{dc} * e^{j \frac{5\pi}{3}}$ |

The space vector diagram for the VSI is shown in Fig.4. The Fig.5 illustrate typical 8-segment sequence for voltage respectively.Generally switching times of switches S1-S6 in six sectors was listed in Table 2.







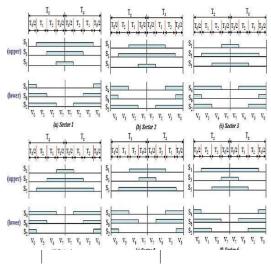
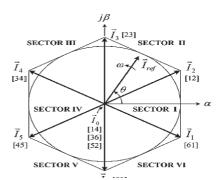


Fig.5 SVPWM switching patterns of all the six sectors Table 2 Switching time calculation at each Sector

B. SVPWM for Current Source Inverter

TheFig.6 shows an idealized current source inverter. It is having six switches and SCR.The equivalent structure for CSI and possible combinations of switching states for CSI is shown in Fig.7



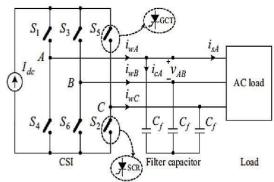


Fig.6Circuit diagram of CSI

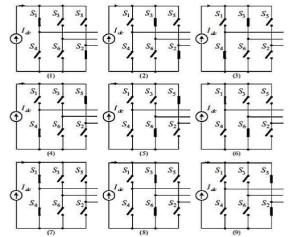


Fig.7 Switching states for a CSI

The PWM switching pattern for the CSI shown in Fig.6 Under this constraint, the switching states as listed in Table 3.

| Table | 3 | Switching | states | for | a | three | phase |
|-------|---|-----------|--------|-----|---|-------|-------|
| CSI | | - | | | | | - |

| Type | Switching | Switching On-state States Switch | | erter P current | | Vector definition | |
|---------------|-----------|-------------------------------------|-----------------|--------------------|-----------------|---------------------------------------------------------------|--|
| | States | Switch | i _{wA} | i _{wB} | i _{wC} | | |
| | [14] | S_1, S_4 | | | | | |
| Null vector | [36] | S_3, S_6 | 0 | 0 | 0 | $\vec{l}_0 = 0$ | |
| | [52] | S_5, S_2 | | | | | |
| Active vector | [61] | S_6, S_1 | Ι _{dc} | $-\vec{l}_{dc}$ | 0 | $\vec{l}_1 = \frac{2}{\sqrt{3}} I_{dc} * e^{-j\frac{\pi}{6}}$ | |
| | [12] | S_1,S_2 | <i>Î</i> dc | 0 | $-\vec{I}_{dc}$ | $\vec{I}_2 = \frac{2}{\sqrt{3}} I_{dc} * e^{j\frac{\pi}{6}}$ | |
| | [23] | S_{2}, S_{3} | 0 | <i>Ī</i> dc | $-\vec{I}_{dc}$ | $\vec{I}_3 = \frac{2}{\sqrt{3}} I_{dc} * e^{j\frac{\pi}{2}}$ | |
| | [34] | S_3, S_4 | $-\vec{I}_{dc}$ | <i>Î</i> dc | 0 | $\vec{l}_4 = \frac{2}{\sqrt{3}} I_{dc} * e^{j\frac{5\pi}{6}}$ | |
| | [45] | S_4, S_5 | $-\vec{I}_{dc}$ | 0 | Ι _{dc} | $\vec{I}_5 = \frac{2}{\sqrt{3}} I_{dc} * e^{j\frac{7\pi}{6}}$ | |
| | [56] | S_5, S_6 | 0 | $-\vec{l}_{dc}$ | \vec{I}_{dc} | $\vec{I}_6 = \frac{2}{\sqrt{3}} I_{dc} * e^{j\frac{9\pi}{6}}$ | |

The SV diagram for CSI is exposed in Fig.8. The **SVPWM** switching patterns at each sector is shown in Fig.9.Generally, the switching time of six switches, was listed in Table 4.Fig.8 Space vector diagram for the CSI



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| $\frac{1}{S_6}$ | $\vec{i}_1 = \vec{i}_2 = \vec{i}_7$, $S_1 = S_1, S_2 = S_1, S_4$ | | Ĩ2 | \vec{I}_3 S_2, S_3 | 79 S5.S2 | | | |
|------------------------------------|--------------------------------------------------------------------------------|------------------------------------|----------------|---------------------------|--------------------------------|--|--|--|
| S6. | S_1 S_1, S_2 S_1, S_4 | | S_1, S_2 | S2.S3 | 55.52 | | | |
| Vg1 | | VRI | | | | | | |
| V _{S2} | | V _{S2} V _{S3} | | | | | | |
| VET | | VEI | | 1 | <u> </u> | | | |
| VES | | ves | - | 1 | <u> </u> | | | |
| Vg6 | T_1 T_2 T_z | V.86 | | | | | | |
| L | T _x Sector 1 | | - | T _s | | | | |
| | 3 1 ₄ 1 ₈ | | - I4 | icctor 2 | 7. | | | |
| S, | S ₃ S ₃ , S ₄ S ₃ , S ₆ | 2 | S3.S4 | 54.55 | 17 S1,S4 | | | |
| VRI | | VSI | | | | | | |
| v _{g 2} | | Vg 2 | | | | | | |
| V 83 V 84 | | V 53 V 54 | | | | | | |
| VSS | | Ves | | | | | | |
| Pro | | Vyn | <i>. T</i> i . | | | | | |
| 1 | T _s | | < '' > | T_s | 4 ° × | | | |
| - | Sector 3 | | | ector 4 | | | | |
| | $\vec{I}_6 \vec{I}_9$ $S_5 S_5, S_6 S_5, S_2$ | | 1. 5.,5. | \vec{I}_1 S_6, S_1 | \overline{I}_8 S_3, S_6 | | | |
| | | | | | 1 13,06 | | | |
| ν _{g1} ν _{g2} | | v_{g1} v_{g2} | | | | | | |
| V.83 | | v _{£3} | | | ⊨ | | | |
| v _{g4} | | vg4 | | | 1 | | | |
| | | V _{g5} V _{g6} | | | i | | | |
| - | T_1 T_2 T_2 | - | \star r_i | T_2 | T_{z} | | | |
| | Upper Switches | | Lower | Switches | - | | | |
| SECTOR | (S_1, S_3, S_5) | | | $S_6.S_2$ | | | | |
| | | | | 0 25 | | | | |
| | $v_{g1} = T_S$ | | vg | $T_{4} = T_{Z}$ | | | | |
| 1 | $v_{g3} = 0$ | | v | $T_{6} = T_{1}$ | | | | |
| | $v_{g5} = 0$ | | | $T_{2} = T_{2}$ | | | | |
| | | | 8 | | | | | |
| | $v_{g1} = T_1$ | | | ₇₄ = 0 | | | | |
| 2 | $v_{g3} = T_2$ | | | | | | | |
| | $v_{g5} = T_Z$ | | $v_{g6} = 0$ | | | | | |
| | | | vs | $T_{2} = T_{S}$ | | | | |
| | | | | | | | | |
| 3 | $v_{g1} = 0$ | | vg | $T_{4} = T_{2}$ | | | | |
| 5 | $v_{g_{3}} = T_{S}$ | | vg | $T_{6} = T_{Z}$ | | | | |
| | $v_{g5} = 0$ | | vg | $T_{12} = T_{11}$ | | | | |
| | | | | | | | | |
| | $v_{g1} = T_Z$ | | v, | $T_{4} = T_{5}$ | | | | |
| 4 | $v_{g3} = T_1$ | | | ₇₆ = 0 | | | | |
| | $v_{g5} = T_2$ | | | ₂₂ = 0 | | | | |
| | vg5 - 12 | | 5 | 12 - 0 | | | | |
| | | | | - T | | | | |
| | $v_{g1} = 0$ | | | $T_{4} = T_{1}$ | | | | |
| 5 | $v_{g_3} = 0$ | | - | $T_{16} = T_2$ | | | | |
| | $v_{g5} = T_{S}$ | | vg | $T_{2} = T_{Z}$ | | | | |
| | | | | | | | | |
| | | | | | | | | |
| | $v_{g_1} = T_2$ | | v_{ξ} | $_{p4} = 0$ | | | | |
| 6 | $v_{g3} = T_Z$ | | | $T_{5} = T_{5}$ | | | | |
| | $v_{g5} = T_1$ | | | ₂ = 0 | | | | |
| | 80 1 | | à | - | | | | |
| I | | | | | | | | |

Fig.9 SVPWM switching patterns at each sector Table 4 Switching time calculation at each Sector

III. SIMULATION DISCUSSIONS

A. Voltage Source Inverter using SVPWM

The simulation waveforms for VSI using SVPWM, where Vab, Vbc, Vca is line to line voltages, Van is line to neutral

of line to line voltage, line to neutral voltage and load current of VSI using

Space vector pulse width modulation as shown below respectively. The specifications of VSI are shown in Table 5.

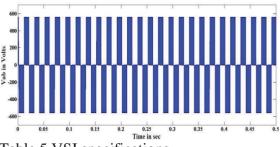


Table 5 VSI specifications

| Modulation | Dc link | Switching | Fundamental | Load | | |
|------------------------|---------------------------|-----------------------|------------------|--------|-------|--|
| Index(m _a) | Voltage(V _{dc}) | Frequency(f_{sw}) | $Frequency(f_0)$ | R(Ohm) | L(mH) | |
| 0.5 | 560V | 6kHz | 50Hz | 10 | 50 | |
| 0.5 | 100V | 20kHz | 100Hz | 10 | | |
| 0.5 | 4004.42V | 450Hz | 50Hz | 20 | 3 | |

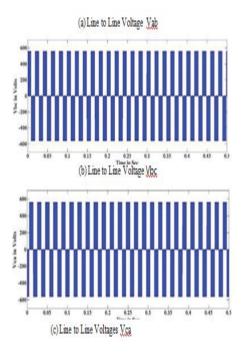


Fig. 10 Line to Line voltages

phase voltage source inverter which are built up of discrete values of voltages of.SVPWM pulses are applied to inverter to produce waveforms shown in Fig.10.

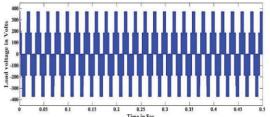
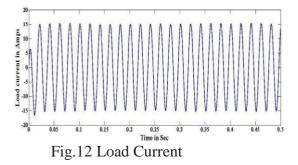


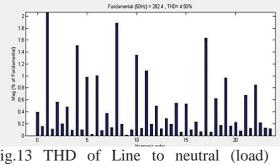
Fig.11 Line to Neutral Voltage for Phase А

The Fig.11 shows the simulated waveform of output voltage by using SVPWM technique. The waveforms of Line to neutral voltage Van which built up of voltage values of -1/3Vdc, -1/3Vdc, 2/3Vdc, 2/3Vdc and 0 according to the switching vectors [3].



The Fig.12 shows load current waveform for voltage source inverter using SVPWM technique for RL load (R = 10Ω and L = 50 mH).

It is observed from the FFT analysis that THD percentage for Line to neutral voltage and Load current of VSI for specifications mentioned above are exposed in Fig.13 and Fig.14which are 4.5 % and 0.85 % respectively [4], [5].





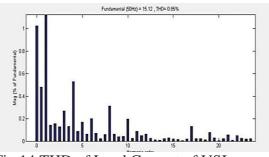


Fig.14 THD of Load Current of VSI Similarly, for specifications of case

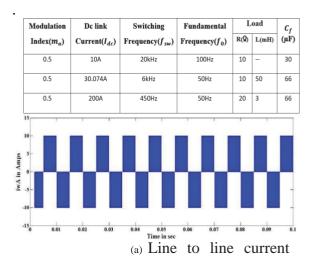
study 2 and 3 given in Table 5 are also simulated same as above and respective THD's are observed.

It is observed from FFT analysis that in case study 2 the THD of line to neutral voltage and load current are 21.03 and 21.03.

It is observed from FFT analysis that in case study 3 the THD of line to neutral voltage and load current are 51.43 and 32.

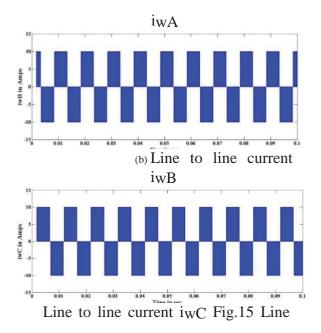
B. Current Source Inverter using **SVPWM**

The simulation waveforms for CSI using Space vector pulse width modulation, where iwa, iwb and iwc line to line currents vab isolated voltage is a is inverter load current. The simulation wave form of line-to-line currents, three phase load currents and three phase load voltage of CSI using SVPWM are exposed below respectively. The specification of CSI is shown in the table 6. Table 6 CSI Specifications



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to line currents iwA, iwB, iwC

Simulated waveforms of line to line currents are iwa, iwb and iwc are generated by three phase current sourse inverter which are build up of discrete values currents of Idc, 0, -Idc. SVPWM pulses are applied to inverter to produce waveforms shown in fig 15

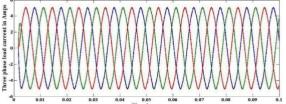
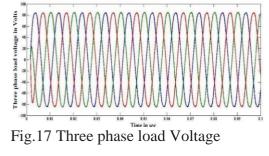


Fig.16 Three phase load current

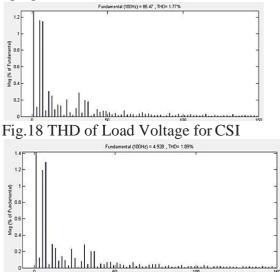
The Fig.16shows the simulated waveform of load current for three phase CSI by using SVPWM technique. The waveform of load current after giving capacitor = 30μ F having R = 10Ω .



| The | Fig.17 | | shows |
|-----------|----------|----|-------|
| simulated | waveform | of | three |

phase load voltage for three phase CSI by using SVPWM technique. The waveforms of load voltage after giving capacitor value = 30μ F having R = 10Ω .

It is observed from the FFT analysis that THD percentage for three phase load voltage and three phase load current for specifications shown in Table 6 are shown in Fig.18 and Fig.19 which are 1.77 % and 1.89 % respectively [7], [10].





Similarly, for specifications of Case study 2 and 3 given in Table 5.2 are also simulated same as above and respective THD (%)'s is observed.

It is observed from FFT analysis that in case study 2 the THD of load voltage and load current are 4.78 and 3.63.

It is observed from FFT analysis that in case study 3 the THD of load voltage and load current are 5.31 and 4.34.The overall simulations on VSI and CSI are presented in the Table 7.

Table 7 Overall VSI and CSI with different specifications



| | | | V _{dc} / | | | | Load | | | I_l/I_{sA} |
|------|-----------|----------------|-------------------|---------------------|----------------------|------------------------|----------|-----------|-----------------------------------------|--------------|
| S.no | Converter | m _a | I _{de} | f ₀ (Hz) | f _{sw} (Hz) | С _f (µF) | R (Ω) | L (mH) | V _{AB} /V _l THD% | THD % |
| 1 | VSI | 0.5 | 560V | 50 | 6kHz | | 10 | 50 | 4.5 | 0.85 |
| 2 | VSI | 0.5 | 100V | 100 | 20kHz | | 10 | | 21.03 | 21.03 |
| 3 | VSI | 0.5 | 4004.42V | 50 | 450Hz | | 20 | 3 | 51.43 | 32 |
| 4 | CSI | 0.5 | 10A | 100 | 20kHz | 30 | 10 | | 1.77 | 1.89 |
| 5 | CSI | 0.5 | 30.074A | 50 | 6kHz | 66 | 10 | 50 | 4.78 | 3.63 |
| 6 | CSI | 0.5 | 200A | 50 | 450Hz | 66 | 20 | 3 | 5.31 | 4.34 |

From the above table, VSI having switching frequency 6 kHz with dc link voltage 560V, fundamental frequency 50 Hz has giving less Load current and load voltage THD when compared to the other two specifications of VSI.

Similarly, in CSI having switching frequency 20 kHz with dc link current 10A, fundamental frequency 100 Hz has giving less Load current and Load voltage THD when compared to the other two CSI specifications.

IV. CONCLUSION

SVPWM is implemented for VSI and CSI, where in the algorithms are discussed and converter topologies are compared in details. The operation of both VSI and CSI is studied with different switching frequencies namely 450 Hz, 6 kHz and 20 kHz and THD results are compared. By observing overall VSI and CSI models with different specifications, all CSI models are providing very less %THD. So the performance of CSI with SVPWM is showing better results when compared to all VSI Models.

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