ANALYSIS OF VARIOUS REVERSIBLE LOGIC GATES USING MENTOR GRAPHICS TOOLS

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Abstract: *The rapid changes in VLSI industry continues to determine a smaller feature size, causing the mixing of many transistors on one piece of chip, as the transistors number on chip increases the power dissipation also increases. It is reduced by Logic gates with reversible technology. A one-to-one relation between inputs & outputs is realized[3] with the help of reversible logic property, all the inputs & outputs are often retrieved from one another . CMOS implementation of varied logic gates using reversible technology is proposed in this paper. Logic gates with reversible technology is becoming one among the most growing design technology having its uses in low-power CMOS, cryptography and nanotechnology[1] . The idea of Logic gates with reversible technology has become vital tool for turning out with economical digital circuits with low-power dissipation.*

Research done in the paper aims to use the retrospective view of reversible logic to interrupt classic speed-power, this may optimize in terms of quantum cost, delay, power dissipation[2],thanks to low power dissipation in computing reversible logic is a beautiful field of research in quantum and optical computing.

Conventional circuits are irreversible in nature and dissipate power for each bit loss in circuit. In this paper we discuss about some Logic gates with reversible technology like Feynman gate, Fredkin gate, Peres gate, Toffoli gate, TR gate. This paper is meant to design and implementation of Logic gates with reversible technology by using mentor graphics backend tools with 130nm technology to beat the Power loss of classic logic gates[4], it's been observed a big decrease in power dissipation, delay compared to classic CMOS logic.

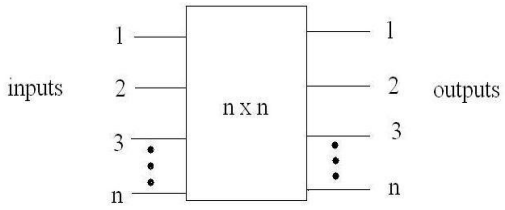
Index Terms-: Logic gates with reversible technology, power dissipation, quantum cost, mentor graphics tool.

I. INTRODUCTION

The changing perspective has got a lot of attention over the years due to their ability to minimize the power supply which is a major requirement for VLSI power generation. Logic circuits with reversible technology have theoretically zero internal power dissipation , since they do not loose information. Reversible computation doesn't require erasing any little bit of information [7]. The circuit actually operates in a reverse direction, allows generating the inputs from the outputs and consumes zero power [1]. It realizes the network connection of given gates with reversible technology and confirm that cost is low, where fan out and feedback aren't permitted [3].

A reversible gate is an n-bit function that connects every input vector to a unique output vector. Reversible computing also will lead in improving overall energy utilization of the design. Significant requirements in making circuits with reversible technology is to reduce gate volume, junk outputs, delays and quantum costs [7].Any reversible circuit must be made with less number of

logic gates with reversible technology, they supply cost effective solution to the exponentially increasing needs of commercial electronics. A basic diagram of reversible gate is shown in below figure



Basic diagram of reversible gate

Characteristics:

1. A reversible gate should have same number of input and output vectors i.e., 2x2,3x3…….n x n.
2. for every input pattern, there must be a unique output pattern.
3. Each output must be used only once [9].
4. Loops and feedbacks aren't permitted in reversible designing.

II.LOGIC GATES WITH REVERSIBLE TECHNOLOGY:

A reversible gate may be a memory-less electronic device that realizes an injective logic function. Here we study the basic properties of Logic gates with reversible technology and circuits, which are needed for further discussion [5]. Reducing the entire amount of garbage signals is a crucial problem in designing reversible logic circuits

Garbage output: The output of the gate, which isn't given as a input of another gate, is referred as junk output. For good performance, number of junk outputs must be minimum [1].

Quantum cost : This refers to the importance of the circuit with respect to primitive gates, i.e., the amount of primitive gates like 1x1 and 2x2 required for the belief of a gates/circuits with reversible technology [2].

1. FEYNMAN GATE:

Feynman gate is a 2x2 one through reversible gate as shown in figure 2.The input vector is I(A,B) and output vector is Q(P,Q).The outputs are defined by P=A,Q=A⊕B. Since the fan-out isn't allowed in reversible logic, this gate is beneficial for duplication of the specified outputs.

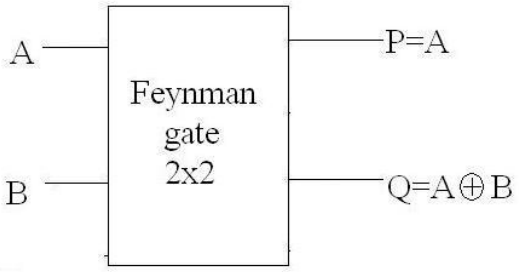


Fig 1: Feynman Gate

Feynman is also named as Controlled NOT gate.

The quantum cost is 1.If B=0 it duplicates the input A and if B=1 then it inverts the input A to the output Q.

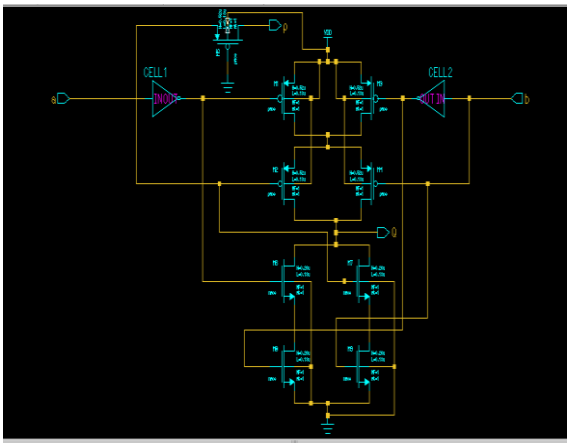


Fig 1(a): CMOS Implementation of Feynman gate

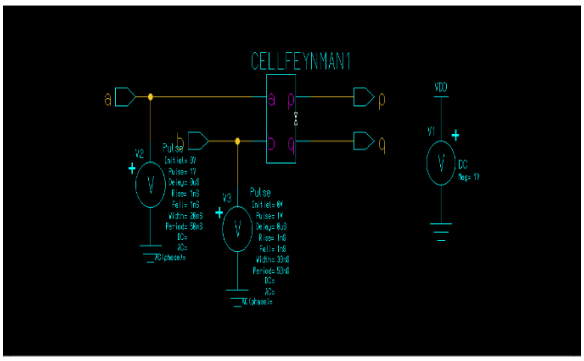


Fig 1(b):symbol depiction of Feynman gate

MODELLING RESULTS:

Here the Feynman reversible gate is modelled by using mentor graphics tool with 130nm technology. Also here we are comparing the parameters like total power dissipation, delay.

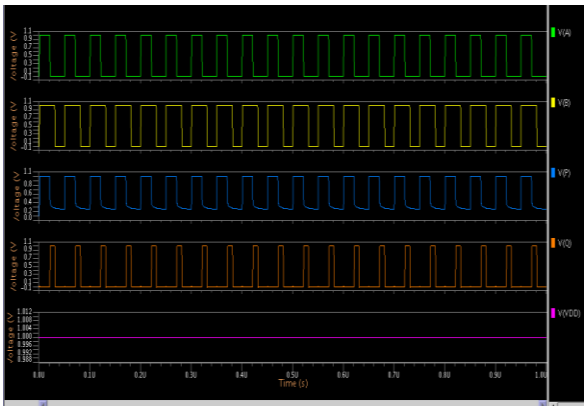


Fig 1(c):modelling result of Feynman gate

2. FREDKIN GATE:

This gate is also named as controlled swap gate. it's a computational circuit suitable for reversible computing, invented by EDWARD FREDKIN. Another 3X3 reversible gate is Fredkin gate, the association between I/O's are often represented by P=A, Q=A'B⊕AC, R=A'C⊕AB.

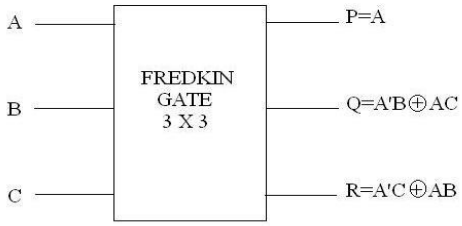


Fig 2: Fredkin gate

Fredkin gate implements as a multiplexer, if the input is either '0' or '1' then the outputs Q and R swaps between the inputs B and C.

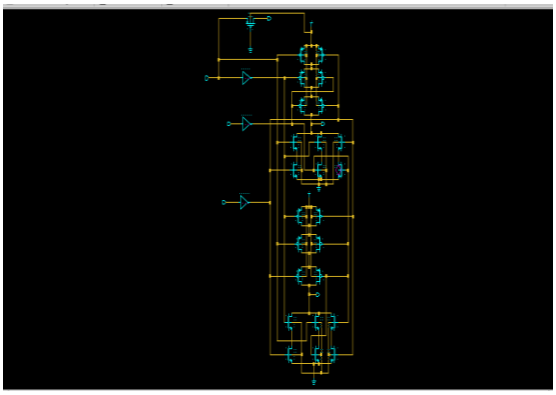


Fig 2(a): CMOS implementation of Fredkin gate

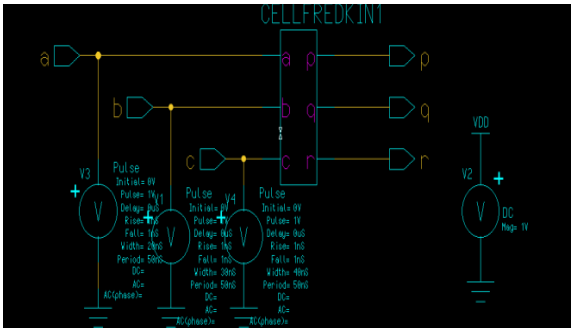


Fig 2(b): symbol depiction of Fredkin gate

MODELLING RESULTS:

Here the Fredkin reversible gate is modelled by using mentor graphics tool with 130nm technology. Also here we are analyzing the parameters like total power dissipation, delay.

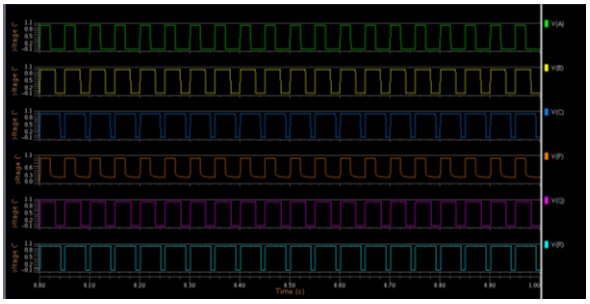


Fig 2(c):modelling result of Fredkin gate

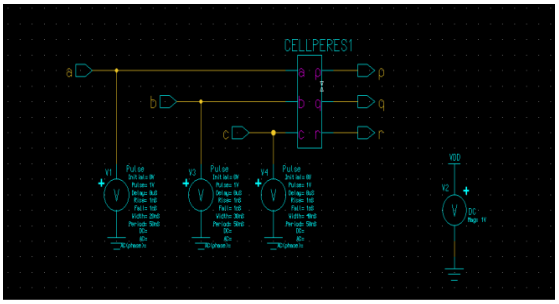


Fig 3(b): symbol depiction of Peres gate

3. PERES GATE:

Peres gate is proposed by ASHER PERES. this is often another 3 X 3 reversible gate. The I/O's are defined as I(A,B,C) and O(P,Q,R) respective. The relation between I/O's is P=A, Q=A⊕B, R=AB⊕C.

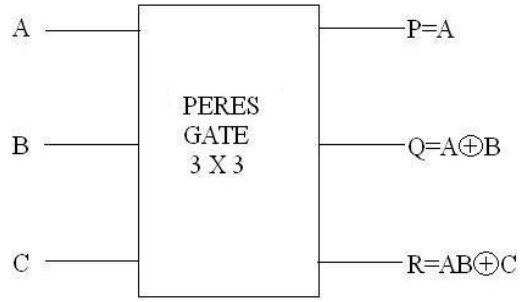


Fig 3: Peres gate

This Peres gate is implemented using few Feynman gate and a NAND circuit .

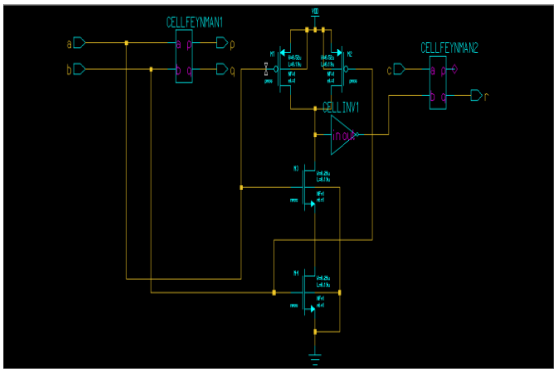


Fig 3(a): CMOS implementation of Peres gate

MODELLING RESULTS:

Here the Peres reversible gate is modelled by using mentor graphics tool with 130nm technology. Also here we are analyzing parameters like total power dissipation, delay.

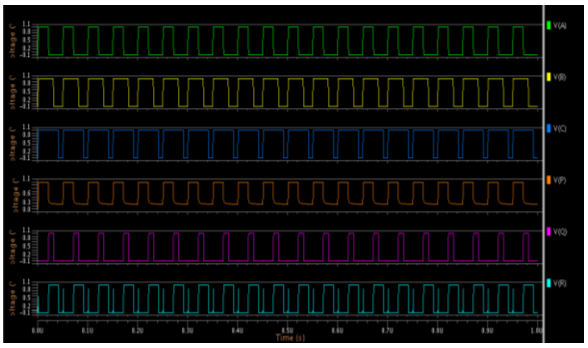


Fig 3(c): modelling result of Peres gate

4. TOFFOLI GATE:

This gate is additionally named as controlled- controlled- not gate. This gate is invented by TOMMASO TOFFOLI, may be a universal reversible gate , which suggests that any reversible circuit are often constructed from Toffoli gate. The connection between inputs I(A,B,C) and outputs O(P,Q,R) can be represented by P=A,Q=B,R=A⊕B.

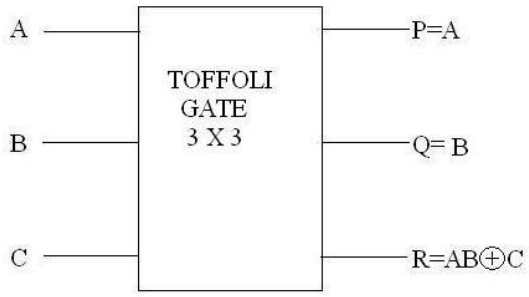


Fig 4: Toffoli gate

It has 3-bit I/O's, if the primary two bits are both set to 1, it reverses the third bit, otherwise all bits stay in previous state value .

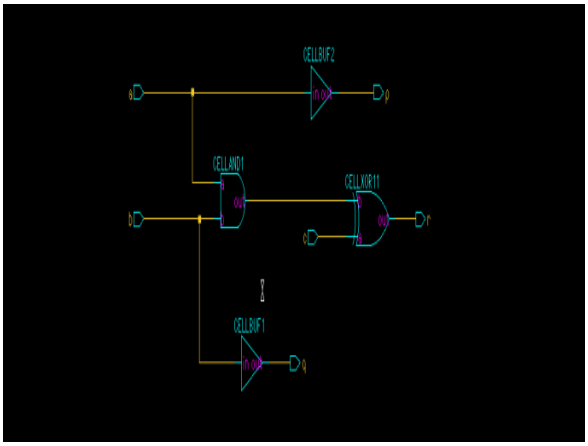


Fig 4(a): schematic of Toffoli gate

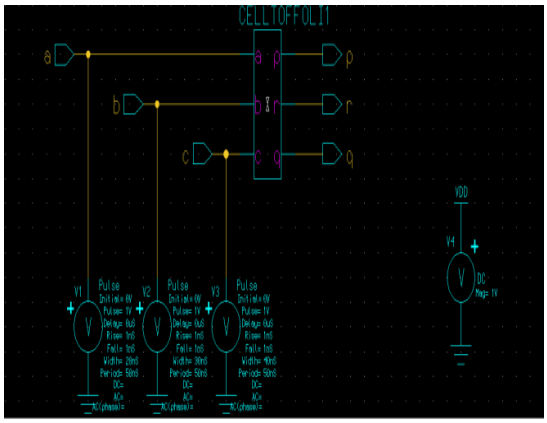


Fig 4(b): symbol depiction of Toffoli gate

MODELLING RESULTS:

Here the Toffoli reversible gate is modelled using mentor graphics tool with 130nm technology. Also here we are comparing parameters like total power dissipation, delay.

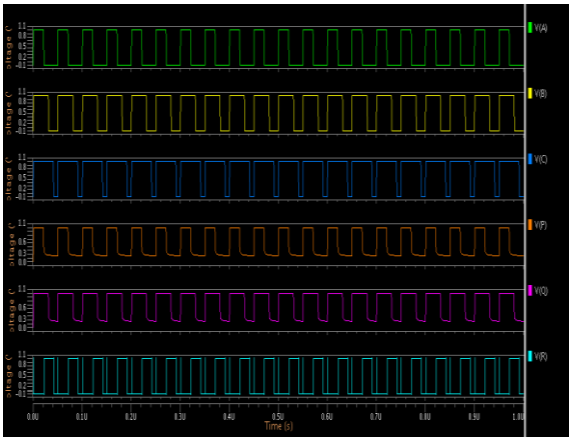


Fig 4(c): modelling results of Toffoli gate

5. TR GATE:

This gate is proposed by TAPLIYAL and RANGANATAN. It has 3-bit I/O's. The I/O's are defined as I(A,B,C) and O(P,Q,R).

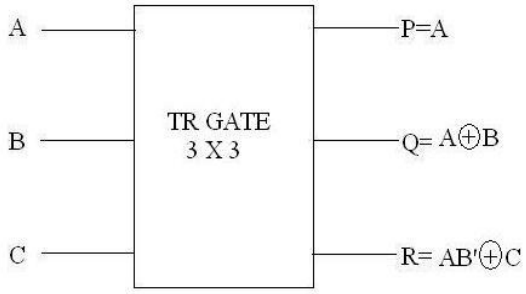


Fig 5: TR Gate

The connection between I/O's is P=A, Q=A⊕B, R=AB'⊕C. This gate has unique one-to-one mapping.

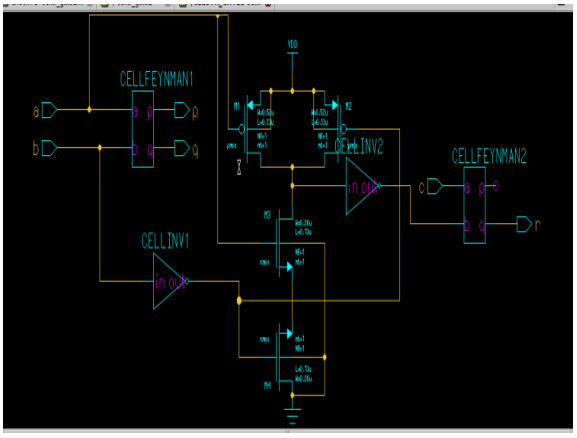


Fig 5(a): CMOS implementation of TR gate

Sl.No.	Reversible Gate	Power Dissipation	Delay
1	Feynman Gate	2.47NWatts	P=A-109.16 ps Q=(A⊕B)-28.819Ns
2	Fredkin Gate	3.6079N Watts	P=A-110.67 ps Q=(A`B⊕AC)-49.77Ns R=(A`C⊕AB)-49.78Ns
3	Peres Gate	5.4010N Watts	P=A-109.65 ps Q=(A⊕B)-28.812Ns R=(AB⊕C)-28.713Ns
4	TR gate	7.3532N Watts	P=A-109.64 ps Q=(A⊕B)-28.818Ns R=(AB`)⊕C-49.875Ns
5	Toffoli gate	7.5880N Watts	P=A-107.87 ps Q=B-58.954Ns R=AB⊕C-30.593Ns

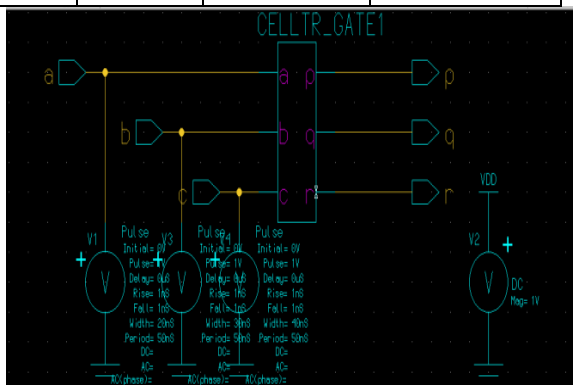


Fig 5(b): symbol depiction of TR gate

MODELLING RESULTS:

Here the TR reversible gate is modelled with mentor graphics tool at 130nm technology. Also here we are comparing parameters like total power dissipation, delay.

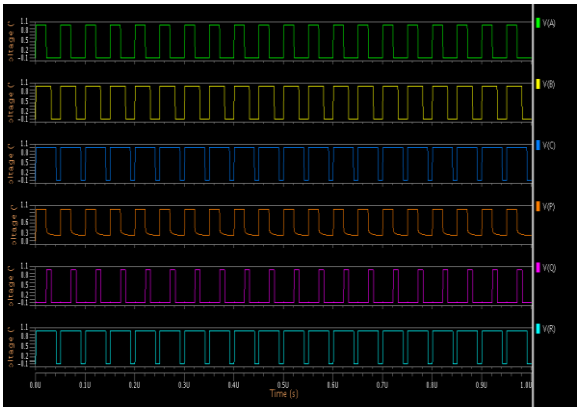


Fig5(c): modelling result of TR gate

Comparison table

III.APPLICATIONS

Reversible computing might have utilizations in many fields, but the main long term benefits will be felt very well in those areas which require high energy efficiency, speed and performance, it includes areas like:

- Low power CMOS.
- Quantum computing.
- Nanotechnology.
- Optical computing.
- DNA computing.
- Computer graphics.
- Communication.
- Field programming gate array (FPGAs) in CMOS technology.

IV.CONCLUSION

The circuits with reversible technology forms the main functional block of quantum computers. This paper implements the basic gates with reversible technology and this paper helps the designers to design more complex computing circuits using gates

with reversible technology. Here, we presented the CMOS implementation of different logic gates using backend tools at 130nm technology. Also we calculated and compared the different parameters which includes total power dissipation, delay and for all gates. Power dissipation is very less for logic gates with reversible technology in comparison with classic logic gates.

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