FULL ADDER ANALYSIS USING FINFET TRANSISTORS

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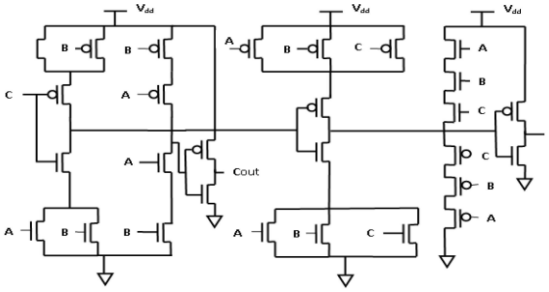
Abstract:
The objective of this paper is to analyze Full Adder circuit using FinFET which solves the problems faced in CMOS circuits. The proposed FinFET based circuit reduce the power consumption. As CMOS circuit performance reduces when fabricated below45nm technology, FinFET devices is the alternative solution. The basic motivation is to Analyze an efficient, fast and low power full adder. Since the basic building block of a multiplier is an adder circuit, a study on the area and the power consumed by different adders was reviewed and a proper relation was found out between power and area complexity of all the adders under consideration.

Keywords: CMOS, FINFET, Leakage current, Power Consumption,

I. INTRODUCTION

Today, number of portable applications requires,a limited amount of available powera small footprint, low power and high performance circuit. Consequently, low power circuits become a major concern for the design of microprocessors and system components. Research effort on low power microelectronics has been stepped up and the low power VLSI systems are appeared excessively in demand. An adder is one of the most vital component of a CPU (central processing unit), an arithmetic logic unit (ALU), a point block and address generation floating like a cache or access block, cell phones, personal digital assistant (PDA) and laptop for staff ,device on the basis of the battery. So the design of a high performance full adder becomes very useful and vital [1]. One of the best known full adder is the CMOS standard full adder, which uses 28 transistors, shown in the fig.1 In this document, we present a complete 1-bit adder circuit using 10 transistors with adequate power consumption and delay characteristics. The main advantages of 10 transistor full adders are, small area compared to full adder with large number of transistors [2], lower power consumption and lower operating voltage. It becomes more difficult and even obsolete to continue operating at full voltage back and forth as you pursue designs with fewer transistors and less power consumption [3]. The pass transistor logic, the output voltage moves back and forth can be graded up in connection with the problem of loss threshold therefore attractive idea is essential for improvement in the overall module performance [4]-[5]. The main disadvantage of 10-transistor full adder is that it suffer from a loss in the threshold voltage of the pass-through transistors. All have double threshold losses at the full adder output terminals [6]. These drawbacks have been overcomed by applying the double gate FINFET method 1Bit full adder Design. There is a need to use areal and energy-efficient VLSI circuits. The DB FINFET has two electrically independent gates, giving circuit designers more design flexibility. Dual gate field effect transistors, referred

as an alternative, to reduce short channel



effects (SCE).

Fig 1.Conventional Full Adder

1-bit FULL ADDER :

In this article we present a complete 1-bit adder circuit , with adequate power consumption, execution latency , and duty cycle . The main advantage of full adder using 10 transistor is its low area compared to that of full count adders for higher gates, low power consumption and low operating voltage. It is becoming increasingly difficult and even obsolete to maintain full voltage forward and reverse operation as designs are developed with fewer transistors and lower power consumption. Reducing the voltage swing is, on the one side, beneficial for energy consumption. On the other side, this can lead to slow switching in the case of cascade operation,such as ripple.

When operating at low VDD, a degraded output signal may even cause circuit failure. Therefore, for structures with low-voltage oscillations, special attention should be given for the stability of power consumption and speed. We need 4 XOR transistors to implement several full 10-titransistor adders. A 2-to-1 multiplexer circuit or circuit with 4 XNOR transistors. The 1-bit full adder circuit is shown in Figure 2.

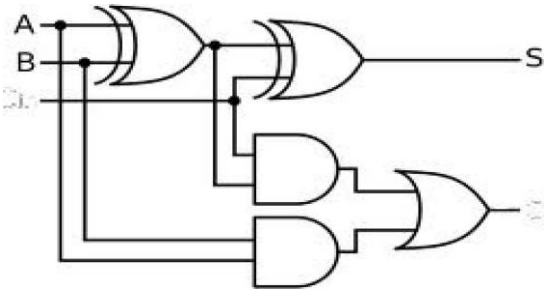


Fig.2. Diagram of 1 bit Full adder

This topology uses a total of 10 transistors to implement the following logical expressions. Consider a complete 1-bit adder. This circuit has two operands, A and B, and an input carry Cin.

II. FINFET

FinFET means Fin Field Effect Transistor. FinFET is a Non Planar Dual Gate Transistor used in the Silicon Architecture which consists of very large computational density. FinFET was coined by Berkeley researchers of university of California and it was developed for the use of Silicon-on-Insulator. FinFET technology takes its name from the fact that the FET structure looks like a set of "fins". The main characteristic of the FinFET is, it has a conducting channel wrapped by a thin silicon "fin".The thickness of the fin determines the effective channel length of the device.

A fin Field Effect Transistor (FinFET) is a multigate device, built on a substrate where the gate is placed on two, three, or four sides of the channel or wrapped around the channel, forming a double gate structure. The FinFET devices have significantly faster switching speed and higher current density than planar CMOS (complementary metal-oxide-semiconductor) technology. Basic

structure of FINFET is shown in Fig: 3.

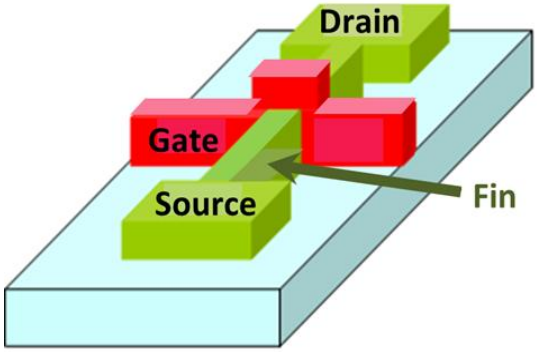


Fig 3. Structure of FINFET

FinFET Structure The attractiveness of FinFET is its 3D structure that rise above the planar substrate giving more volume than a planar gate for same planar area. This gate electrode operates on a single transistor. In contrast to a Planar the source and Drain channel is built by three dimensions on the top of the silicon substrate called as Fin. MOSFET FinField Effect techniques are promising substitutes for bulk CMOS at nanoscale.

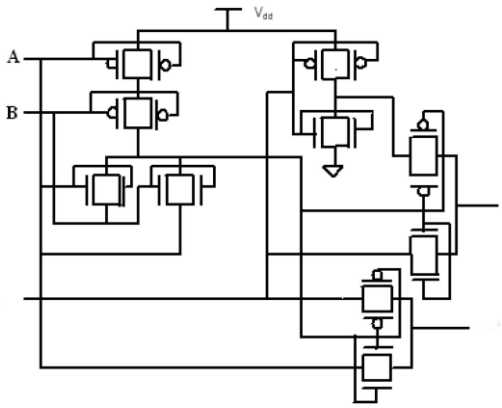
The main advantage of FinFET full adder is Low cost, suppressed Short channel effects and Better in Driving current. In digital circuits, Full adders are used extensively. The performance of 1-bit full adder using FinFET is benchmarked against conventional CMOS full adder. The FinFET based full adder shows a large reduction in delay and provided the device with high speed performance which is better than the conventional CMOS Full Adder. The FinFET has better and faster switching speed due to the presence of multiple gates in the FinFET structure and drives more current compared to MOSFET structure.

III. 1-Bit Full Adder Using CMOS & FINFET

The FINFET double-gate method is applied in the 1-bit full adder design. Here, the self-detecting front and rear door controls in DG FinFET can be effectively used to increas e performance and reduce power consum ption . On non-critical paths, self-determining gate control can be used to connect transistors in parallel. A second gate was added opposite the conventional gate in double gate FINFETS (DG), which was predictable due to its short channel effects, forward-looking and superior control as well as leakage current control. FINFET operations are recognized as a short gate (SG) mode with connected gates of a transistor, an independent gate (IG) mode in which self-determined digital signals are used to drive two of the device's gates, a low power mode and an optimum power mode where the tailgate i s connected to reverse bias voltage to red uce the power leakage and hybrid mode, i n which the arrangement of the shutter m odes of low power works and is itself defi ning.

Critical barriers to a scaling of CMOS bel ow 45nm are gate dielectric leakage current a nd the optimum variations Over short channel device structures. FinFET offer excellent control over short channel effects, low leakage a nd better performance at 45 nm which hel p to overcome scaling obstacles.

The DG FINFET circuit used in the 1-bit full adder is shown in Figure4. Figure5 shows the 1-bit full adder Output waveform using the FINFET method.



result can be measured using the CADENCE VIRTUOSO tool.

IV. CONCLUSION

Fig 4. 1-bit FinFET full adder

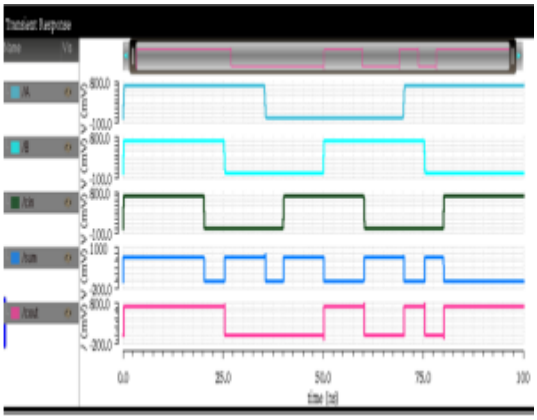


Fig 5. Waveforms of 1-bit FinFET full adder

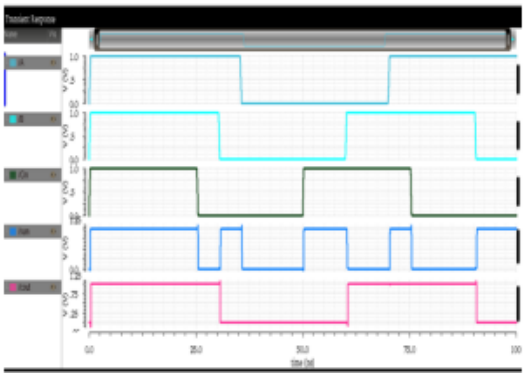


Fig.6 Waveforms of 1-bit CMOS full adder

Digital CMOS - circuit may have three main sources of energy dissipation , namely , the dynamic power , short circuit and leakage. A 1-Bit Full Adder based on the FINFET method has been proposed. Analysis of the simulation results confirm that the applicability of the FINFET method in the design of full adder shows that the power dissipation parameter is 25-30% less than the CMOS method with a supply voltage of 0.7 V. In general, we achieve minimum power dissipation. The simulation We investigated on the performance and parameters of the circuit , as the operationg current, a current leakage and the leakage power related to 1 Bit Full Adder using a FinFET in cadence virtuous 45nm. The advantage of having the same functionality with very few transistors will be useful when performing an 1bit full adder.Mobility is improved in devices with high ribs due to increased tensile stress . We were also rated duty cycle of 96.56%, which is approximately 2 times higher than the CMOS 1 Bit full adder.

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