ANALYSIS AND COMPARISON OF REVERSIBLE HYBRID FULL ADDER/FULL SUBTRACTOR AND CONVENTIONAL FULL ADDER & FULL SUBTRACTOR

K.VENKATESWARLU
ASST.PROFESSOR,
ECE,MIST

S.KIRPAL KOUR
ASST.
PROFESSOR,ECE,MIST

Dr.JASPAL KUMAR
PROFESSOR &
HOD,ECE,MIST
jaspalkumar@rediffmail.com

Abstract:
Logic gates with reversible technology will be implemented over a high scale in the future technologies. Reversible logic is seen as demanding field with the variegated applications like CMOS design consuming less power. Reversible computation plays an important role in low power circuit design and efficient energy recycling[4] . A reversible logic gate which has the equal number of inputs and outputs and one-to-one mapping between the input vectors, so that the input vector states can be uniquely reconstructed from the output vector states. This paper includes a reversible full adder/subtractor design with logic gates using reversible technology and produces less number of junk outputs. The main purpose of designing logic gates with reversible technology is to decrease the quantum cost, depth of the circuits and the number of junk outputs[5] . Thus the proposed architecture of hybrid full adder/subtractor is having minimum number of junk outputs than the existing architecture.
Reversible full adder is further used in the construction of n-bit full adder/subtractor. An adder is a VLSI application used in ALU design, address generation in processors, multiplexers and so on. The complexity in VLSI design increases with increasing level of integrity. In conventional CMOS design the area, power dissipation and delay are more when compared to low power technique, reversible logic[1]. Adders is a versatile component and mainly used in addition and multiplication based on the basic processing element.
The reversible circuits are building block of quantum computers , since the operations involved in this are reversible. In this paper we proposed a design of full adder using logic gates with reversible technology. The design of full adder is modelled by using mentor graphics tool with 130nm technology and also here we compared the parameters like power dissipation, delay between convention full adder/subtractor and reversible full adder/subtractor[2] .

KEY WORDS: Logic gates with reversible technology, adder, subtractor, mentor graphics tool, low power.

I. INTRODUCTION

Reversible circuits always maintain one-to-one mapping between inputs and outputs, and is performed by logic gates with reversible technology [6]. Some outputs in reversible circuits are neither used in further stages of computation nor restore any original inputs. These redundant outputs are called junk outputs. Adders are one of the most important blocks of the digital applications. In this paper we designed one bit hybrid full adder by using different logic gates with reversible technology [11]. Generally this full adder circuits are implemented using CMOS logic, it has an important characteristics i.e., high noise immunity but there is a significant increase in the power consumption due to the increasing speed and complexity of the circuit.

Reversible logic is becoming prominent technology for low power applications [7]. Logic gates with reversible technology can produce exclusively same input vector from each output vector and vice versa. A computation will be said to be reversible if the inputs can be generated from outcomes. There are irreversible computations that dissipates heat a highly important source of computational resource is energy [10].In this paper we implemented Hybrid Full adder/subtractor using different logic gates with reversible technology. We used two Peres gates and two Feynman gates [7]. Reversible logic has wide variety of applications in the field of emerging technologies such as quantum computers, optical computing, cellular automata, ultra-low power VLSI. Block diagram of logic gates with reversible technology is shown in below figure 1.

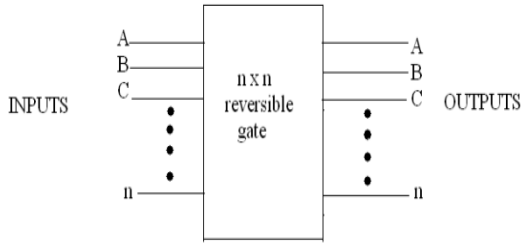

Fig 1: logic gate with reversible technology

II. LOGIC GATES WITH REVERSIBLE TECHNOLOGY:

We have a lot of logic gates with reversible technology for low power consumption. In that we choose Feynman gate, fredkin gate, peres gate, TR gate [7]. The selected logic gates with reversible technology are low cost and simple in design.

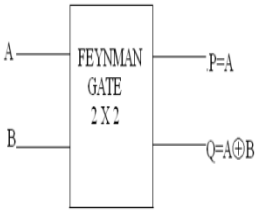

Fig2 (a): Feynman gate

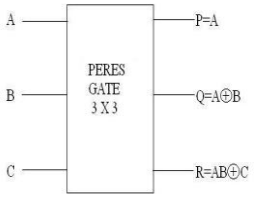

Fig2 (b): Peres gate

Fig2: Few preferred reversible gates

III. HYBRID FULLADDER/SUBTRACTOR DESIGN:

A full adder is defined as circuit that takes two input bits a carry- in bit and produces the outputs sum and carry-out. One bit reversible hybrid adder/subtractor using two Feynman gates and two peres gates is shown in figure in 3a.

A control input is given to switch between adder and subtractor[3]. If control input is '0' addition operation is performed else if it is '1' subtractor is performed.

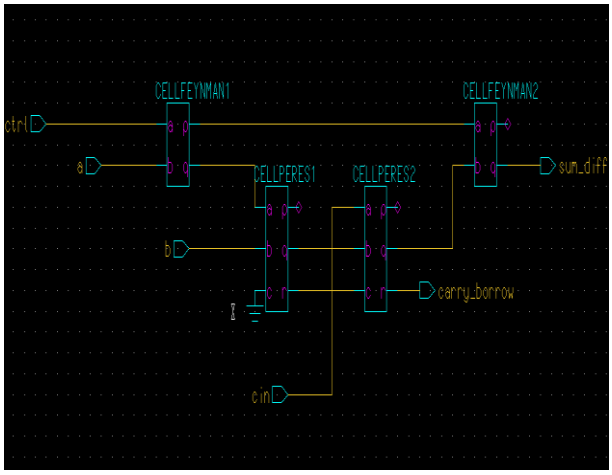

Fig3(a): realization of full adder/subtractor

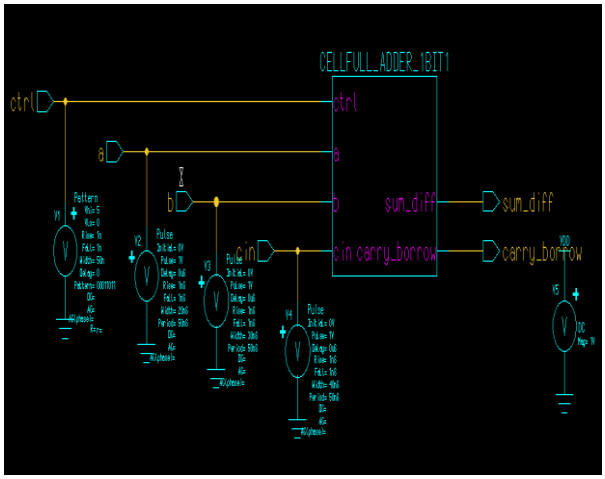

Fig3(b):symbol representation of hybrid full adder/subtractor

COMPARISION AND MODELLING RESULTS:

Here the hybrid full adder/subtractor design are modelled by using mentor graphics tool with 130nm technology, also we are comparing parameters like delay and total power dissipation.

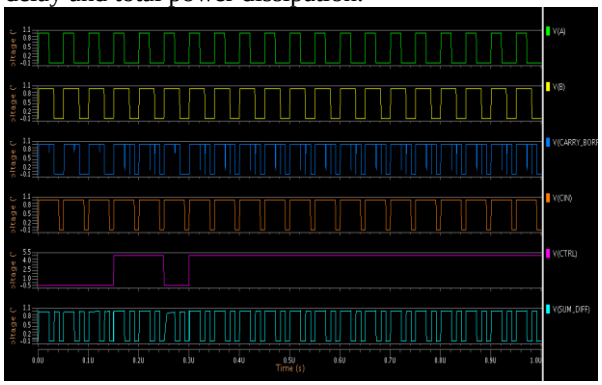

Fig3(c): modelling result of full adder/subtractor design

IV.FULL ADDER and SUBTRACTOR USING NORMAL GATES:

FULL ADDER: In which the adder which adds three inputs and produces two outputs. The first two inputs are A and B and third input is input carry as C-in and the two outputs are sum and carry [5].
Full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to another.

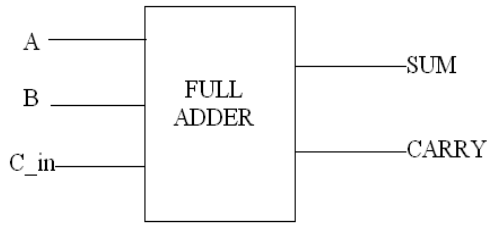

Fig4: block diagram of full adder

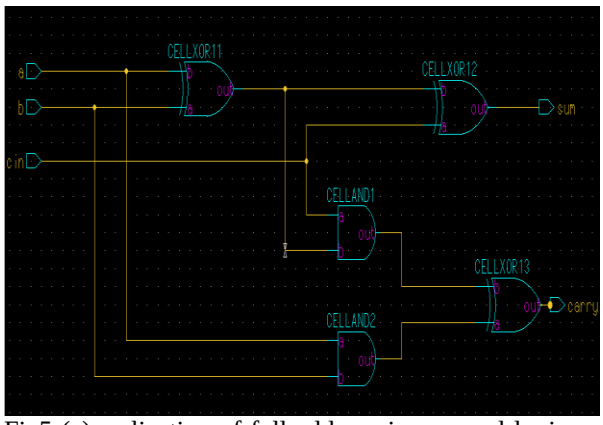

Fig5 (a):realization of full adder using normal logic gates.

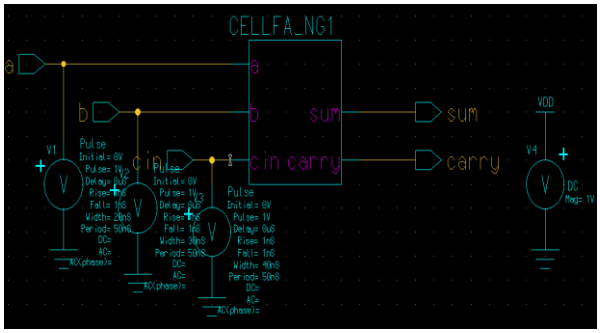

Fig5 (b):symbol representation of full adder

MODELLING RESULTS:

Here the full adder using normal gates is modelled by using mentor graphics tool with 130nm technology, also we are comparing the parameters like delay and total power dissipation.

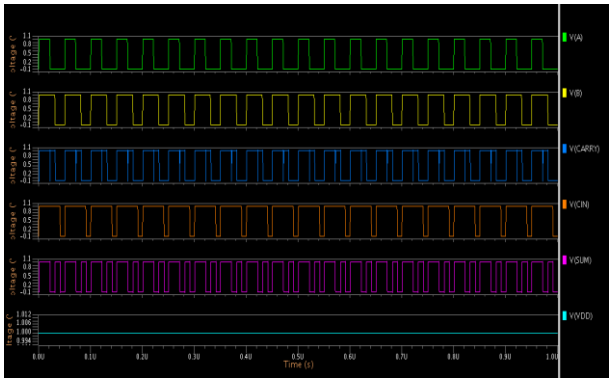

Fig5(c): modelling result of full adder

FULL SUBTRACTOR:

A Full subtractor can perform subtraction of two bits, one is minuend and other is subtrahend, taking into account borrow of the previous adjacent lower minuend bit[11]. The circuit has three inputs and two outputs. The three inputs A, B, Bin, denote the minuend, subtrahend, previous borrow. The two outputs, D and Bout represent the difference and outputs borrow.

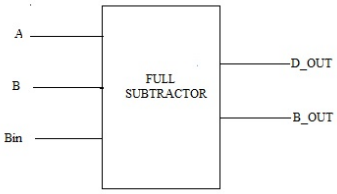

Fig 6: Block diagram of full subtractor

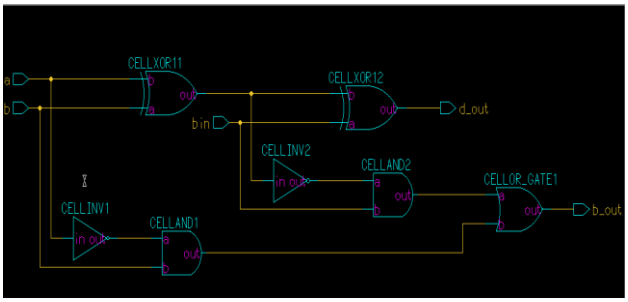

Fig6(a): realization of full subtractor using normal gates.

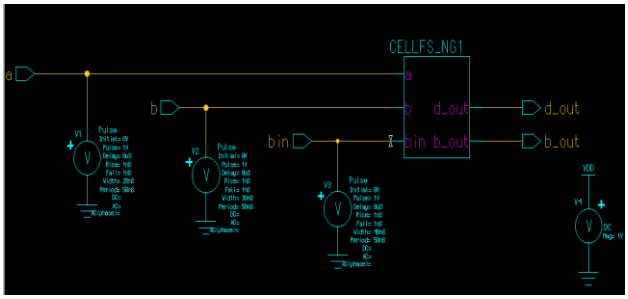

Fig6(b): symbol representation of full subtractor

MODELLING RESULTS:
Here the full subtractor using normal gates are modelled by using mentor graphics tool with 130nm

technology, also we are comparing the parameters like delay and total power dissipation.

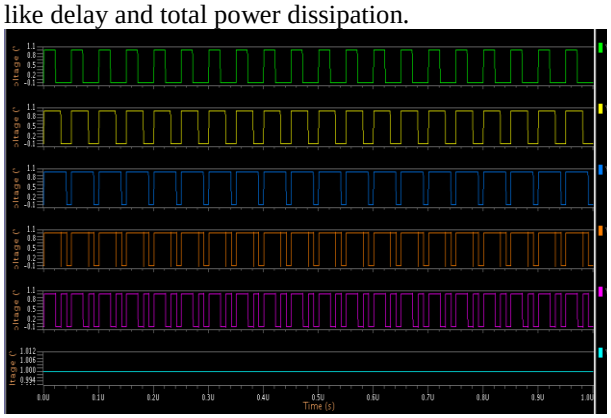

Fig6(c): modelling result of full subtractor

COMPARISON TABLE:

Parameter	Hybrid Full adder/subtractor using reversible gates	Conventional full adder/subtractor
Power dissipation	38.0720NWatts	43.5603NWatts
Delay	Sum=(A,B,C)= 15.731 Ns C-out=(A,B,C)= 52.6335 Ns	(SUM/DIF-(A,B,C)) =31.5563 Ns C_out/B_out(A,B,C) =31.3393 Ns

APPLICATIONS:

- Quantum computing
- Nanotechnology
- Optical computing
- Computer graphics

V.CONCLUSION:

In this paper we implemented the hybrid full adder/subtractor using reversible logic and conventional logic gates. By comparing the parameters like power dissipation and delay we conclude that hybrid Full adder/subtractor using logic gates with reversible technology is beneficial.

In the future we can work for the power consumption for the fault tolerant full adder and full subtractor. Here we used different logic gates with reversible technology to implement full adder using mentor graphics tool with 130nm technology, also we calculated and compared delay, total power dissipation. It has been observed that the power dissipation is less for reversible full adder/subtractor compared to Conventional one.

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