FLEXIBLE CONTROL SCHEME FOR A DYNAMIC VOLTAGE RESTORER FOR POWER-QUALITY IMPROVEMENT

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Abstract

This paper presents the control framework dependent on the supposed tedious control for a five-level flying-capacitor dynamic voltage restorer (DVR). This DVR staggered geography is appropriate for medium-voltage applications and worked by the control conspire created in this paper. It can moderate force quality unsettling influences, for example, voltage lists, symphonious voltages, and voltage lopsided characteristics all the while inside a transfer speed. The control structure has been partitioned into three subsystems; the first improves the transient reaction of the channel used to wipe out the balance high-recurrence music, the subsequent one arrangements with the heap voltage; and the third is accused of keeping up adjusted voltages in the flying capacitors. The all around created graphical offices accessible in PSCAD/EMTDC are utilized to do all demonstrating parts of the dreary regulator and test framework. Reproduction results show that the control approach performs adequately and yields astounding voltage guideline.

Keywords— power quality, DVR, UPQC, voltage sags, overvoltage, harmonics voltage compensation, FACTS.

I. Introduction

Power quality (PQ) has become an important issue over the past two decades due to the relentless integration of sensitive loads in electrical power systems, the disturbances introduced by nonlinear loads, and the rapid growth of renewable energy sources. Arguably, the most common PQ disturbance in a power system is voltage sags, but other disturbances, such as harmonic voltages and voltage imbalances[2], may also affect end user and utility equipment leading to production downtime and, in some cases, equipment terminal damage.

The dynamic voltage restorer (DVR) is one of the most efficient and economic devices to compensate voltage sags .The DVR is basically a voltage-source converter in series with the ac grid via an converters are normally used and, therefore, much of the published interfacing transformer, conceived to mitigate voltage sags and swells . For low-voltage applications, DVRs based on two-level literature on DVRs deals with this kind of converter. Nevertheless, for higher power applications, power-electronic devices are usually connected to the medium-voltage (MV) grid and the use of two-level voltage converters becomes difficult to justify owing to the high voltages that the switches must block.

One solution is to use multilevel voltage-source converters which allow high power-handling capability with lower harmonic distortion and lower switching power losses than the two levelConverter. Among the different topologies of multilevel converters, the most popular are: neutral-point-clamped converters(NPC),flying-capacitor converters (FC), and cascaded-multimodular or H-bridge converters. NPC converters require clamping diodes and are prone to voltage imbalances in their dc capacitors

A DVR has to supply energy to the load during the voltage sags. If a DVR has to supply active power over longer periods, it is convenient to provide a shunt converter that is connected to the DVR on the DC side. As a matter of fact one could envisage a combination of DSTATCOM and DVR connected on the DC side to compensate for both load and supply voltage variations. In this section, we discuss the application of DVR for fundamental frequency voltage...

The voltage source converter is typically one or more converters connected in series to provide the required voltage rating. The DVR can inject a (fundamental frequency) voltage in each phase of required magnitude and phase. The DVR has two operating modes

(i)Standby (also termed as short circuit operation (SCO) mode) where the voltage injected has zero magnitude.

(ii)Boost (when the DVR injects a required voltage of appropriate magnitude and phase to restore the Pre fault load bus voltage).

The major objectives are to increase the capacity utilization of distribution feeders (by minimizing the RMS values of the line currents for a specified power demand), reduce the losses and improve power quality at the load bus. The major assumption was to neglect the variations In the source voltages. This essentially implies that the dynamics of the source voltage is much slower than the load dynamics.

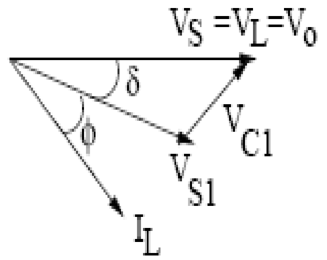
When the fast variations in the source voltage cannot be ignored, these can affect the performance of critical loads such as (a) semiconductor fabrication plants (b) paper mills (c) food processing plants and (d) automotive assembly plants. The most common disturbances in the source voltages are the voltage sags or swells that can be due to (i) disturbances arising in the transmission system, (ii) adjacent feeder faults and (iii) fuse or breaker operation. Voltage sags of even 10% lasting for 5-10 cycles can result in costly damage in critical loads. The voltage sags can arise due to symmetrical or unsymmetrical faults. In the latter case, negative and zero sequence components are also present.

II. CONTROL STRATEGY

There are three basic control strategies as follows.

1. Pre-Sag Compensation

The supply voltage is continuously tracked and the load voltage is compensated to the pre-sag condition. This method results in (nearly) undisturbed load voltage, but generally requires higher rating of the DVR. Before a sag occur, VS = VL = Vo. The voltage sag results in drop in the magnitude of the supply voltage to VS1. The phase angle of the supply also may shift . The DVR injects a voltage VC1 such that the load voltage (VL = VS1 + VC1) remains at Vo (both in magnitude and phase). It is claimed that some loads are sensitive to phase jumps and it is necessary to compensate for both the phase jumps and the voltage sags.

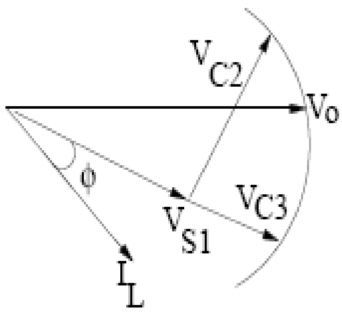


2. in-phase Compensation

The voltage injected by the DVR is always in phase with the supply voltage regardless of the load current and the pre-sag voltage (Vo). This control strategy results in the minimum value of the injected voltage (magnitude). However, the phase of the load voltage is disturbed. For loads which are not sensitive to the phase jumps, this control strategy results in optimum utilization of the voltage rating of the DVR. The power requirements for the DVR are not zero for these strategies

3. Minimum Energy Compensation

Neglecting losses, the power requirements of the DVR are zero if the injected voltage (VC) is in quadrature with the load current. To raise the voltage at the load bus, the voltage injected by the DVR is capacitive and VL leads VS1. Fig.the in-phase compensation for comparison. It is to be noted that the current phasor is determined by theload bus voltage phasor and the power factor of the load.



Implementation of the minimum energy compensation requires the measurement of the load current phasor in addition to the supply voltage. When VC is in quadrature with the load current, DVR supplies only reactive power. However, full load voltage compensation is not possible unless the supply voltage is above a minimum value that depends on the load power factor.

III. CONTROLLER PARAMETERS

The parameters of the control systems for the LC output filter and the load voltage have been calculated from the values of the copper loss resistance, the leakage inductance, and the capacitor Cf Using MATLAB. The cutoff frequency of the LC filter is 2 kHz. Hence, the computed matrix gain that is necessary to obtain this cutoff frequency $\mathbf{K} = [k_i \; k_u] = [150.30 \; 0]$ is and, with reference to (3), it is shown that this design implies that there is no need to measure the LC-filter output voltage.

In order to design the regulator $R(s)$, , based on the repetitive control, the parameter ω_1 was chosen to be $\omega_1 = 2\pi f_1 = 100\pi$ rad\s while the cutoff frequency of the second-order Bessel filter $Q(s)$ was set at 4 kHz. The filter has a linear phase lag on its pass band that is equivalent to a constant time delay of . The Bode diagram of the transfer function $G(s)$: the system has zero gain at frequencies and guarantees the closed-loop system stability since it exhibits a phase margin that is equal to PM=34.8 deg at a gain crossover frequency $\omega_0 = 17.8 \cdot 10^3$ rad\s, and a gain margin GM=2.91 dB at a phase-crossover frequency $\omega_u = 23.3 \cdot 10^3$ rad/s. The Bode diagram of $G_u(s)$ is also provided, showing that the control system eliminates the resonance peak that the LC filter exhibits.

The Bode diagrams of the closed-loop transfer functions $F(s)$ and $F_w(s)$, respectively. As Fig. 7 shows, perfect tracking of the reference input with zero phase is achieved within a bandwidth. Furthermore, the transfer function $F_w(s)$ has zero gain at the fundamental frequency and its harmonics within a bandwidth.

Finally, the amplitude of the added square-wave signal D, used in the general law (16) to control the flying-capacitor voltages, was set at 80 V for each converter leg.

IV. Matlab model

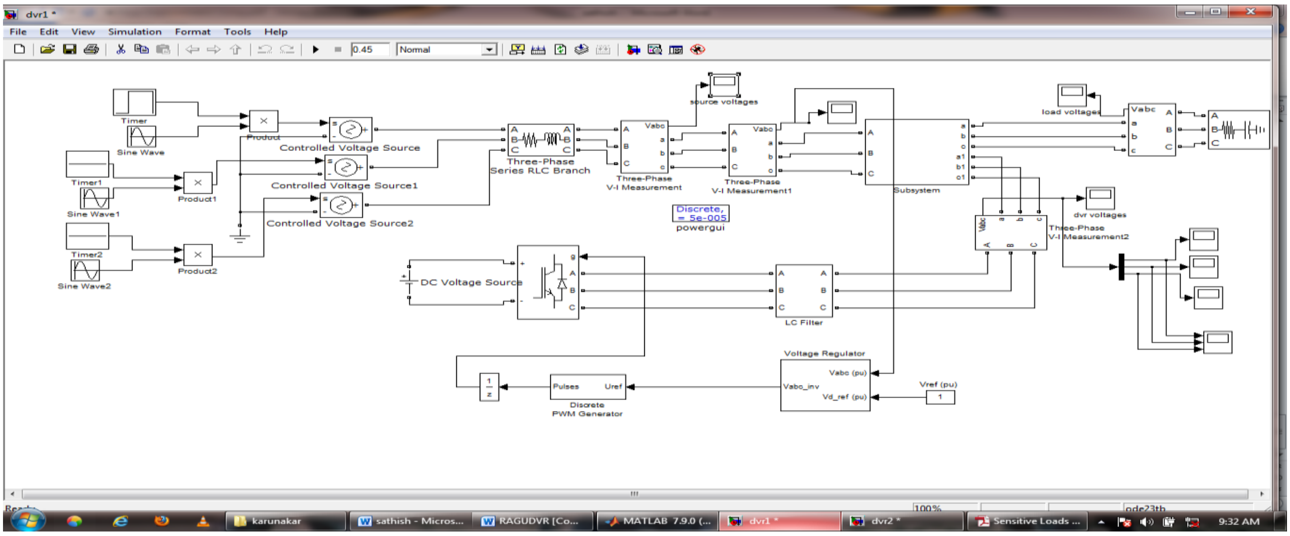
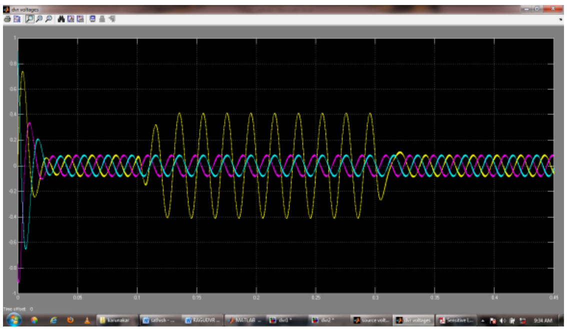
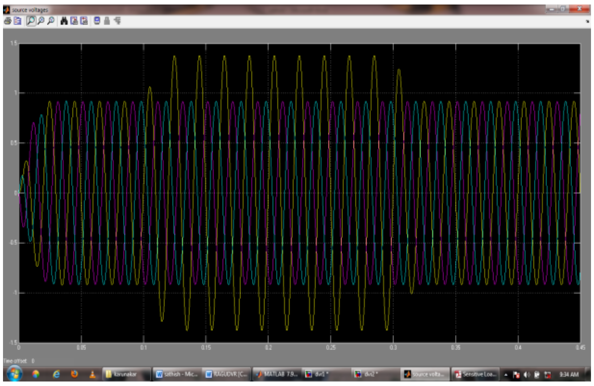


Fig.1.Simulink model of the proposed circuit

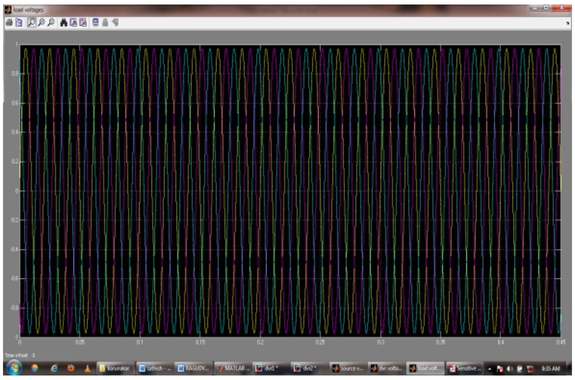
Figure 2(a) shows a sagof 75% between 0.1s and 0.3s on two phases of the supply voltage. The DVR must operate to correct this fault in order to obtain a stable, proper andeffective load voltage to protect figure 2(c). This intervention is made by the injection of a compensation voltage through an injection or coupling transformer connects this series circuit with the network (Figure 2 (b)).



(b) DVR Voltages



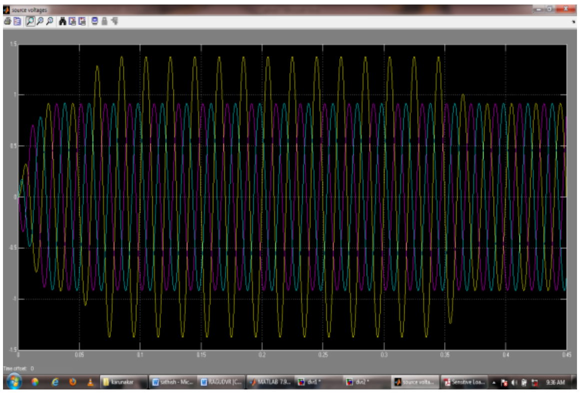
(a) Sorce Voltages



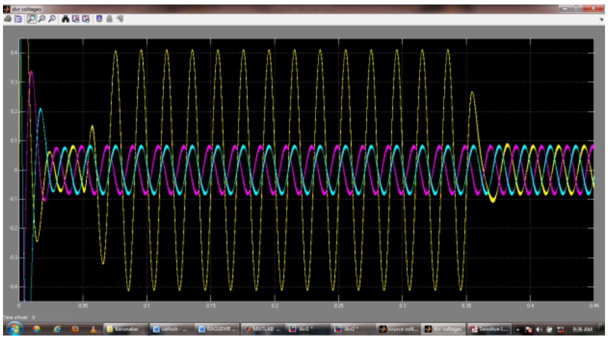
(c) Load Voltages

Fig.2. Voltages of Sorce, DVR, Load voltages.

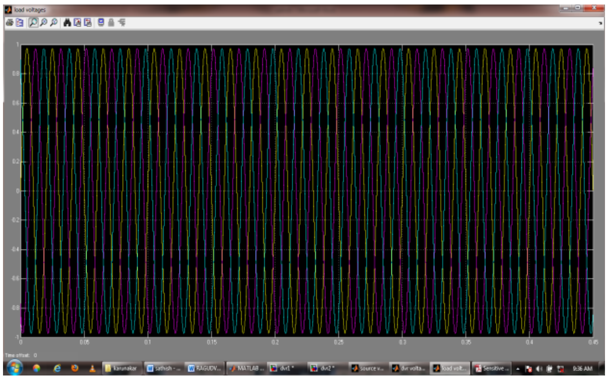
The overvoltage compensation defect is presented in figure 3(a). From times 0.1s to 0.3s, the DVR injects an equivalent power, synchronized but in opposition to that presented by this defect to eliminate it figure 3(b)



(a) Sorce Voltages



(b) ***DVR Voltages***.



(c) Load Voltages

Fig.3. Voltages of Sorce,DVR,Load

V. Conclusion

In this paper, the vast majority of the voltage unsettling influences in low voltage conveyance frameworks have been reenacted MATLAB/SIMULINK programming. Its trademark and execution when applied to a reproduced power framework has been considered. The DVR handles both variety of voltage circumstances with no troubles and infuses the proper voltage part right any peculiarity in the stock voltage to keep the heap voltage adjusted and consistent at the ostensible worth. On account of the abundancy varieties, the DVR infuses a positive part to lessen voltage hangs, and a negative segment contrary to a voltage swell, the two segments are equivalent to the source voltage in every one of the three stages. For the unsettling influence conditions like the voltage changes (Flicker), the DVR infuses a proper uneven voltage segment positive or negative on whether the condition is lopsided voltage list or unequal voltages well. The recreated DVR created, works effectively without needs its exhibition when applied to a reenacted power framework organization.

References

[1] *C. Benachaiba& B. Ferdi, Voltage Quality Improvement Using DVR,Electrical Power Quality and Utilization, Journal Vol. XIV, No. 1, 2008.*

[2] *M. Ali.Taghikhani& A. Kazemi, A New Phase Advanced Multiloop Control System for Dynamic Voltage Restorer", International Journalof Emerging Electric Power Systems, Vol.3, Issue2, Article 1072, 2005.*

[3] *S.V Ravi Kumar & S. Siva Nagaraju, Simulation of D-STATCOM and DVR in Power Systems, ARPN Journal of Engineering and AppliedSciences, Vol.2, NO.3, ISSN 1819-6608, JUNE 2007.*

[4] *Fan Ng, Man-Chung Wong, Ying-Duo Han, Analysis and control of UPQC and its DC-link power by use of p-q-r instantaneous*

power theory, IEEE Power Electronics Systems and Applications, ProceedingsFirst International Conference, 9-11 Nov.2004, pp:43-53

[5] *A. Rai& A. K. Nadir, Modeling & Simulation of Dynamic Voltage Restorer (DVR) for Enhancing Voltage Sag, Sensors & TransducersJournal, Vol. 87, Issue 1, pp. 85-93, January 2008.*

[6] *Y. Y. Kolhatkar& S. P. Das, An Optimum UPQC with Minimum VA Requirement and Mitigation of Unbalanced Voltage Sag, InternationalJournal of Emerging Electric Power systems, Vol.2, Issue2, 2005*