IMPLEMENTATION AND ANALYSIS OF CONVOLUTION ENCODER ON FIELD PROGRAMMABLE GATE ARRAY

PUJARI SRIDHAR
Research Scholar,
Jain University, Bengaluru,
Karnataka, India.
Affiliation: Mist, Hyderabad
sridharpujari1234@gmail.com

DR.C.R. BYRAREDDY
Professor Bit
Bengaluru, Karnataka,India
Affiliation :BIT,Bengaluru

Abstract:

In the latest and modern digital communication systems like Software Define Radio (SDR), convolutional encoder is an essential device as an efficient channel coding block in the transmitter and Viterbi decoder at the receiver. The Data transmission over the wireless channel is very much affected by interference, distortion and attenuation that reduces Signal strength there by affects the ratio of Signal to Noise (SNR) which is the main issue factor in communication and hampers the receiver's capacity to receive the transmitted data with minimal errors. Various techniques are there to detect the errors and these errors are corrected so as to limit the rate of occurrence of error (BER). Special channel coding methods called Forward error correction (FEC) which has the capability to encode the data before sending to the channel. Convolution encoder is an efficient coding technique which is used during transmission for space and wireless systems. The main essential feature of convolutional coding is that it can be adopted to a block of data or to a data stream . This paper briefs an architecture which reduces the silicon area complexity and encode processing time as compared to conventional methods. The Verilog coding for the proposed encoder is written, simulated and synthesized using Xilinx ISE version 14.7 tool

1. Introduction:

Communication systems plays a major role in our life, people use cell phones, satellites, internet and data transmission. All these systems are used in an environment with noise sources, also the data might be transmitted for long distances. These effects could cause changes in data values causing data corruption and loss. To overcome this problem channel coding is used which enables to detect and correct the errors at the receiver by decoding using proper decoders such as Viterbi decoder . In channel coding technique, the redundancy bits are added so as to identify the errors occurred and correct them at the receiver successfully. The channel coding is divided into two main types Block codes and Convolutional codes. These codes are differentiated by the absence and the presence of memory in the encoders. In many communication systems, the message symbol bits arrive serially rather than in large blocks, so that the usage of a buffer leads to adding extra hardware .

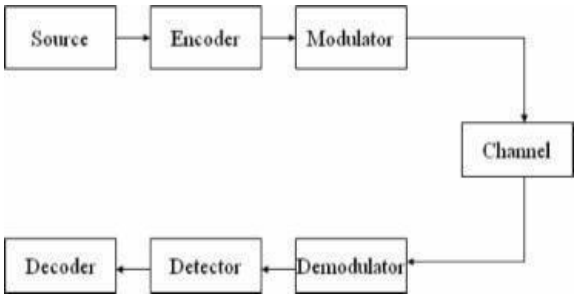

Fig.1.1 Basic block diagram of digital communication system with encoder (convolution encoder) and decoder

In such an environment, the use of convolutional coding may be the best option. The encoder adds extra bits known as redundant bits by using ex-or operation (modulo-2) operation. This encoder (Convolutional codes) are mainly defined using two constants: code rate and constraint length. The code rate(r) as k / n is a count of bits in the convolution encoder (k) to the no of symbols generated by channel of the convolutional encoder (n) in the encoding cycle. The parameter of constraint k denotes length of the convolutional encoder and indicates that many k bits stage are existing to give the combination logic producing the output symbols.

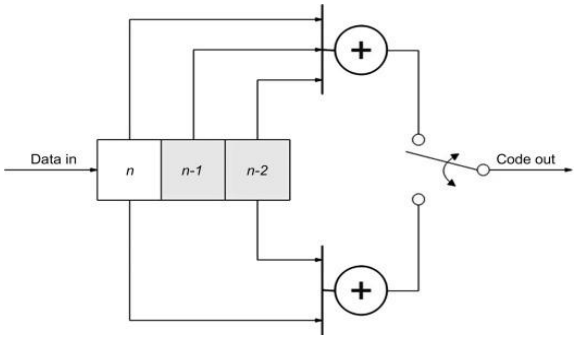

Fig 1.2: (2,1,3) Convolution Encoder

The diagram which describes all the states and their transitions for the above convolution encoder is as in fig.1.3. Each and every state (00,01,10 and 11) are written inside a circle and the change from one state to another is drawn using a line and an arrow. Over the line the input/output code bits are indicated. The encoding implementation can be done by reasonably simple hardware.

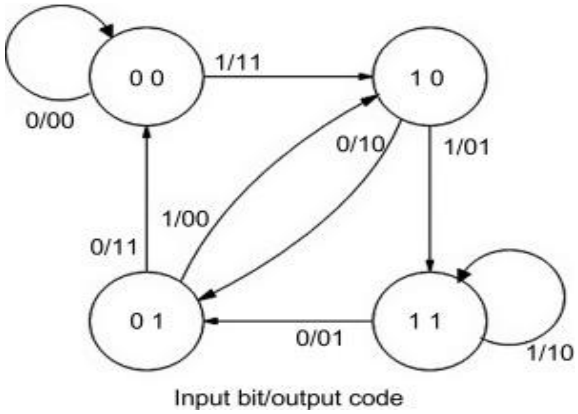

Fig. 1.3 Encoder state diagram

2. Encoder implementation:

In the encoded data the code rate of value is found by using the shifting data at the register to register and output data encryption. Here shift register along with modulo-2 adders are used to encrypt the data (input bit stream).

Memory states	Output (C1)	Output (C2)
100	1	1
010	1	0
101	0	0
010	1	0
101	0	0
010	1	0
101	0	0
010	1	0

Table 2.1 A Byte of message Encoded

Input bit stream :10101010.

Output bit stream:11 10 00 10 00 10 00 10.

The convolution algorithm procedure is as follows:

Step 1:- Initially, to choose the message bit in the input side at current state and previous state bits to save the number.

Step 2:- By shifting the bits, current state during register to register level and calculation of C1 and C2 using XOR operation . This process is repeated up to the change of the message bits.

Step 3:- In the convolutional encoder most likely encoded by the message bit to change from every predecessor state of the Input bits.

Time	Input Bits	Output Bits	Encoder Bits
0	1	1 1	0 0
1	0	1 0	1 0
2	1	0 0	0 1
3	0	1 0	1 0
4	1	0 0	0 1
5	0	1 0	1 0
6	1	0 0	0 1
7	0	1 0	1 0

Table 2.2: Result showing the working of a (2, 1, 3) Convolutional Encoder for a byte of information

A Byte of message bits is encoded by the encoder.

Input :10101010.

Output:11 10 00 10 00 10 00 10.

The Convolutional Algorithm Steps shown in figure 2.1.

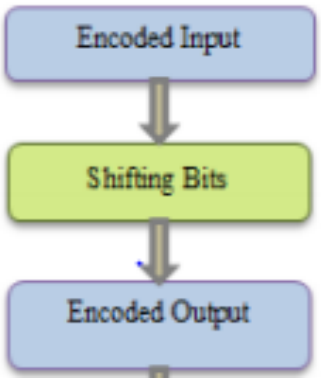

Fig 2.1: Convolutional Encoder Design Flow

Input	Present state	Next state	Output
0	00	00	00
1	00	01	11
0	01	10	11
1	01	11	00
0	10	00	10
1	10	01	01
0	11	10	01
1	11	11	10

Table 2.3: State Table

Trellis Diagram

The trellis diagram is constructed by listing up all the possible states in the vertical axis. Then connect each of the present state to the next by the acceptable code words for that state. Since the code is in binary form there are only two choices likely at each state. These are determined by the arrival of either the bit 0 or the bit 1. The Trellis diagram is the depiction of state diagram of the encoder by a time line i.e. to represent each time unit with a separate state diagram as shown in figure 2.2.

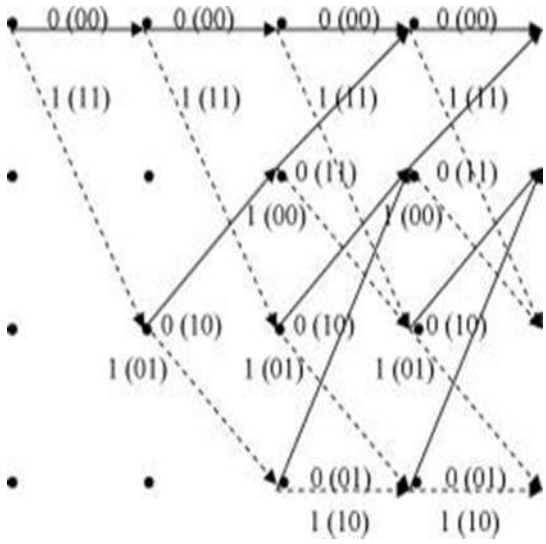

Fig 2.2: The trellis diagram for (2, 1, 3) convolutional encoder

3. Synthesis Report and Result Analysis:

The proposed encoder architecture was designed and tested for simulation results on MATLAB R2016a for different constraint lengths and got the plot for BER as in fig.3.1.The hardware circuit is implemented using Verilog coding and synthesized by Xilinx ISE version 14.7 tool. The RTL schematic of the proposed convolution encoder is as in Fig.3.2.

BER (Bit Error Rate) Analysis

BER is examined to obtain the best suitable circuit so that the hardware can be configured with different constraint lengths.

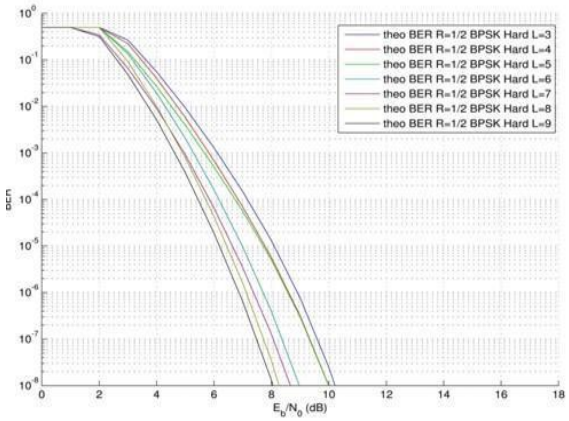

Fig.3.1:Comparison with different constraint lengths

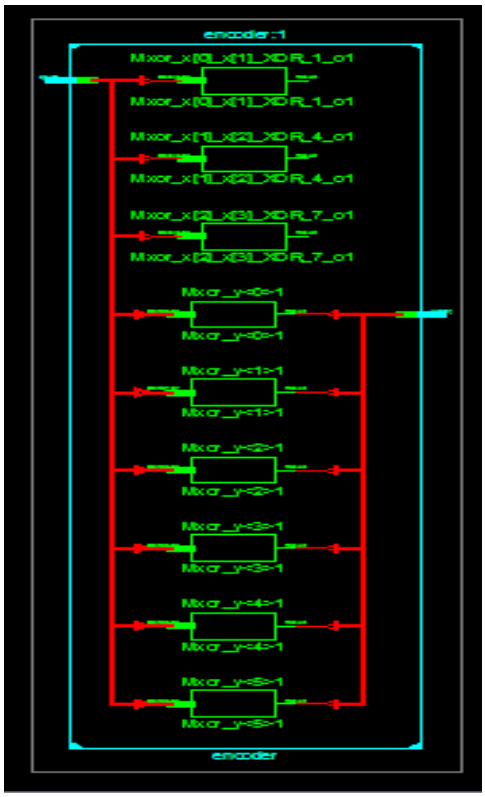

Fig 3.2: RTL Schematic of Convolution Encoder

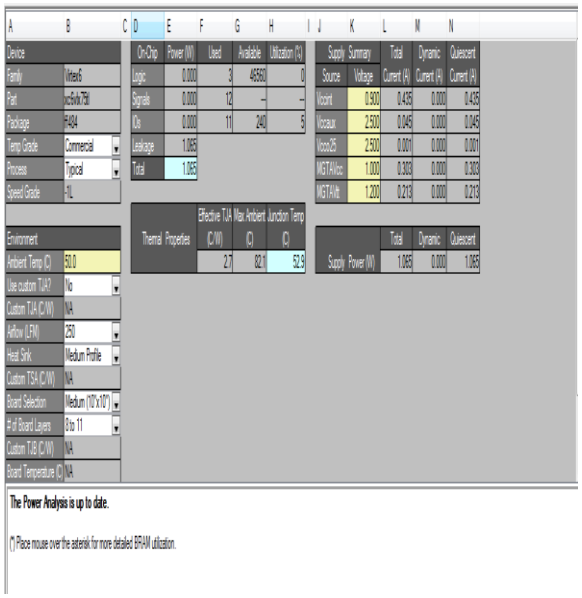

Fig 3.3: Power Report of Convolution Encoder

4. Conclusion:

Convolutional encoder plays a vital role in the field of telecommunication. To implement this design , Verilog HDLcoding is used. The total process is tested on FPGA Virtex-6 Kit. The total power consumed by encryption module is 1.065 W. The total delay in convolutional encoder is 3.597ns both gate and net delays.The BER analysis is done using MATLAB and found that for a constant BER, the circuit with poly2trellis(3,[7,5]) has the best performance. This indicates to have an encoder circuit with three memory elements and g2= (111) and g1= (101) as their impulse response.For applications such as medical image data analysis and in Software Define Radio (SDR), this algorithm secures the data as well as transmits data with minimal errors. New methodologies can help this algorithm in future to diminish the noise activity while keeping up the adequate level of security.

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