A BRIEF STUDY ON INTEGRATED POWER ELECTRONICS MODULE

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ABSTRACT:

Power electronics uses semiconductor technology to convert and control electrical power. Demands for efficient energy management, conversion and conservation, and the increasing take-up of electronics in transport systems has resulted in tremendous growth in the use of power electronics devices such as Insulated Gate Bipolar Transistors (IGBT's). The packaging of power electronics devices involves a number of challenges for the design engineer in terms of reliability. For example, IGBT modules will contain a number of semiconductor dies within a small footprint bonded to substrates with aluminum wires and wide area solder joints. To a great extent, the reliability of the package will depend on the thermo-mechanical behavior of these materials. This paper details a physics of failure approach to reliability predictions of IGBT modules. It also illustrates the need for a probabilistic approach to reliability predictions that include the effects of design variations. Also discussed are technologies for predicting the remaining life of the package when subjected to qualification stresses or in service stresses using thermo-mechanical behavior.S

KEYWORDS: *power electronics, Insulated Gate Bipolar Transistors (IGBT's), thermo-mechanical behavior, thermo-mechanical behavior*

INTRODUCTION:

In power electronics, solid-state electronics is used for the control and conversion of electric power .The goal of power electronics is to realize power conversion from electrical source to an electrical load in a highly efficient, highly reliable and cost effective way. Power electronics modules are key units in a power electronics system. These modules contain integration of power switches and associated electronic circuitry for drive control and protection and other passive components. During the past decades, power devices underwent generation-by-generation improvements and can now handle significant power density. On the other hand power electronics packaging has not kept pace with the development of semiconductor devices. This is due to the limitations of power electronics circuits. The integration of power electronics circuit is quite different from that of other electronics circuits. The objective of power electronics circuits is electronics energy processing and hence require high power handling capability and proper thermal management.

Most of the currently used power electronic modules are made by using wire-bonding technology. In these packages power semiconductor dies are mounted on a common substrate and interconnected with wire bonds. Other associated electronic circuitries are mounted on a multilayer PCB and connected to the power devices by vertical pins. These wire bonds are prone to resistance, parasitic and fatigue failure. Due to its two dimensional structure the package has large size. Another disadvantage is the

ringing produced by parasitic associated with the wire bonds.

To improve the performance and reliability of power electronics packages, wire bonds must be replaced. The researches in power electronic packaging have resulted in the development of an advanced packaging technique that can replace wire bonds. This new generation package is termed as 'Integrated Power Electronics Module' (IPEM). In this, planar metalization is used instead of conventional wire bonds. It uses a three-dimensional integration technique that can provide low profile high-density systems. It offers high frequency operation and improved performance. It also reduces the size, weight and cost of the power modules.

The basic structure of an IPEM contains power semiconductor devices, control/drive/protection electronics and passive components. Power devices and their drive and protection circuit is called the active IPEM and the remaining part is called passive IPEM. The drive and protection circuits are realized in the form of hybrid integrated circuit and packaged together with power devices. Passive compo The commonly used power switching devices are MOSFETs and IGBTs. This is mainly due to their high frequency operation and low on time losses. Another advantage is their inherent vertical structure in which the metalization electrode pads are on two sides.

Usually the gate source pads are on the top surface with non-solderable thin film metal Al contact. The drain metalization using Ag or Au is deposited on the bottom of chip and is solderable. This vertical structure of power chips offers advantage to build sand witch type 3-D integration constructions.

LITERATURE REVIEW:

Canras Batunlu, 2014: Energy is vital for continual progress of human civilization. Accessing to low-cost, environmental friendly, renewable energy sources are keys to economic future for developing countries and around the globe. Wind energy systems are one of the most adequate option where power electronic converters are used for monitoring and conditioning the energy flow; however operating environmental conditions such as variable wind speed cause temperature fluctuations that derive degradation and failures in these systems. Therefore, proper thermal management and control are necessary to monitor their reliability and lifecycle. Besides, power capacity of these devices is being increased by new technological improvements such as multichip designs. Meanwhile, the heat path through the devices has also become more complex due to the heat coupling effect among several chips and it is not possible to be estimated by conventional methods found in literature. In this paper, a three dimensional finite element model (FEM) is implemented for accurate estimation of thermal profile of a power module. Based on the thermal characteristic obtained by the FEM, an electro thermal model was developed to predict the temperatures of each layer of the power module that cannot be measured during service. The work is essential as it solves massive heat transfer issues and it is important to provide health

management of power electronics embedded in wind systems.

Christian Martin, 2004: Due to high current commutation speed, it has become necessary to minimize stray inductances to reduce over voltage. This is a great challenge for the power converter designer. Integration of converters into ever smaller packages decreases stray inductance considerably but at the same time increases other phenomena (thermal issues and EMC disturbances) capable of decreasing reliability and efficiency of the system. This work presents a generic equivalent cabling model and examines the impact of parasitic inductance on current distribution imbalance. This study could therefore be used in thermal analysis in order to better understand the influence of packaging.

C. Buttay, 2007: This paper presents a compact integrated power electronic module (IPEM) which seeks to overcome the volumetric power density limitations of conventional packaging technologies. A key innovation has been the development of a substrate sandwich structure which permits double side cooling of the embedded dies whilst controlling the mechanical stresses both within the module and at the heat exchanger interface. A 3-phase inverter module has been developed, integrating the sandwich structures with high efficiency impingement coolers, delink capacitance and gate drive units. Full details of the IPEM construction and electrical evaluation are given in the paper.

F.C. Lee, August 2004: Assemblies of power semiconductor switches achieved to some extent, the number of interconnects and their associated drive circuit are at present available in modules. Upward into the multi kilowatt range, mixed mode module construction is used. This incorporates monolithic, hybrid, surface mount and wire bond technology. However, a close examination of the applications in motor drives and power supplies indicates that there has been no dramatic volume reduction of the subsystem. The power semiconductor modules have shrunk the power switching part of the converter, but the bulk of the subsystem volume still comprises the associated control, sensing, electromagnetic power passives (inductors, transformers, capacitors) and interconnects. This paper addresses the improvement of power processing technology through advanced integration of power electronics. The goal of a subsystem in a module necessitates this advanced integration, incorporating active switching stages, EMI-filters and electromagnetic power passives into modules. The central philosophy of the technology development research in the National Science Foundation Engineering Research Center for power electronic systems is to advance the state of the art by providing the concept of integrated power electronics modules (IPEMs) for all these functions. The technology underpinning such an IPEM approach is discussed. The fundamental functions in electronic power processing, the materials, processes and integration approaches and future concepts are explained.

Bsoul, 2014: Power gating is an effective technique to reduce static power consumption in integrated circuits. One of the important challenges in power gating architectures is the wakeup current that results from activating blocks in the design after their idle periods end. This wakeup current, also known as inrush current, may cause malfunction of the design. Although solutions exist in power-gated application-specific integrated circuits (ASICs) for this problem, these solutions are fixed and not suitable for reconfigurable devices such as field-programmable gate arrays (FPGAs). In reconfigurable devices, an application is mapped to the device in the field, which means that there is not enough information about inrush current requirements when the chip is fabricated. In this paper we propose a configurable architecture that limits inrush current in power-gated reconfigurable architectures to a safe level. The proposed architecture is configurable to satisfy the inrush current requirements that different applications may experience during the activation phase of power-gated modules. We investigate the different tradeoffs associated with the proposed architecture. Our results show that the area and power overheads of the proposed inrush current limiting architecture are negligible.

ELECTRICAL EQUIVALENT CIRCUIT FOR POWER MODULE:

When faced with the electrical modeling of such complex 3D geometries as those used in power modules, the PEEC method has already shown its great efficiency in computing parasitic inductances, and providing electrical equivalent circuits. However, once all interconnections of the module (DBC, bonding, PCB for gate drive, power lead frame…) have been meshed and replaced by their equivalent circuit, the electrical modeling becomes very complex: several thousands of inductances, with associated coupling. This detailed electrical circuit must be simplified to be used in an electrical simulator.

Four MOSFET chips make up this module. Only the power part will be detailed to explain our modeling method. The gate circuit will not, therefore, be represented hereafter. The same method can, of course, be used to study control disturbances if necessary.

The first model is the simplest. The electrical equivalent circuit for a module accounts for the parasitic impedance with a simple series inductance. This rough representation does not give any information about current division between paralleled chips, or about drive circuit disturbance. This model is often used to estimate voltage surges. This representation is not sufficient if disturbance on the gate circuit is to be found or cabling effect on the module is to be analyzed more accurately. As an alternative to this "compact" representation, an electrical equivalent circuit can be provided, very close to the module geometry: each segment of the layout is modelled by an inductance (and coupling). This presents the great advantage for the designer of knowing exactly where he must act, if the module does not behave as desired. This "quasi-geometric" representation does not allow objective

comparison between several modules, since the number of inductances can obviously be different, if the chip implantation is not the same. Finally an electrical equivalent circuit is chosen, based on the number of terminals of the module. This "input-output" based representation is a concept similar to the Scattering matrix in microwave theory. The global cabling is seen as a multipole, ensuring connections between all chips and the external pins of the module. Three steps are necessary to build this model. Firstly, all input-output terminals electrically connected together are identified. Next, a terminal is arbitrarily chosen as a reference for this connection. Finally, impedances are computed between this reference and all others points of the copper link. These three steps must be repeated for each electrical connection.

In the example of Fig. 1, three pins can be identified connecting to the external circuit (for the power part only): D1, S2 and S1-D2. In the same way each die is made up of two terminals (drain and source) linked either by collector, by emitter or by output phase terminal. Thus, there are eleven terminals to be considered. Fig. 2-c shows the obtained equivalent circuit: both drains are linked to D1, both sources to S2 and other terminals to S1-D2. It is important to notice that all coupling is of course taken into account but not represented on the graph.

Thus, any power module with the same number of chips and the same external pins (e.g. emitter, collector, gate, "clean" emitter, "clean" collector) will be represented by the same electrical equivalent circuit.

An automatic interface between PEEC modeling and SABER has been written, in order to generate a hyper block (a "connection" template), which can be used very easily in Saber sketch. The power module geometry is completely modelled, and the components have just to be connected to this electrical representation.

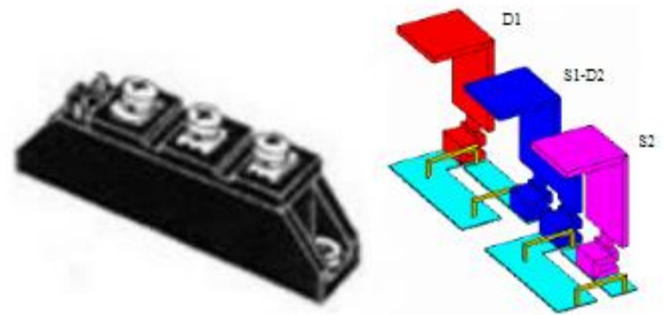

Figure 1. Example of IRFK2D450 MOSFET module (inverter leg) and PEEC modeling of the internal lead frame (power part only)

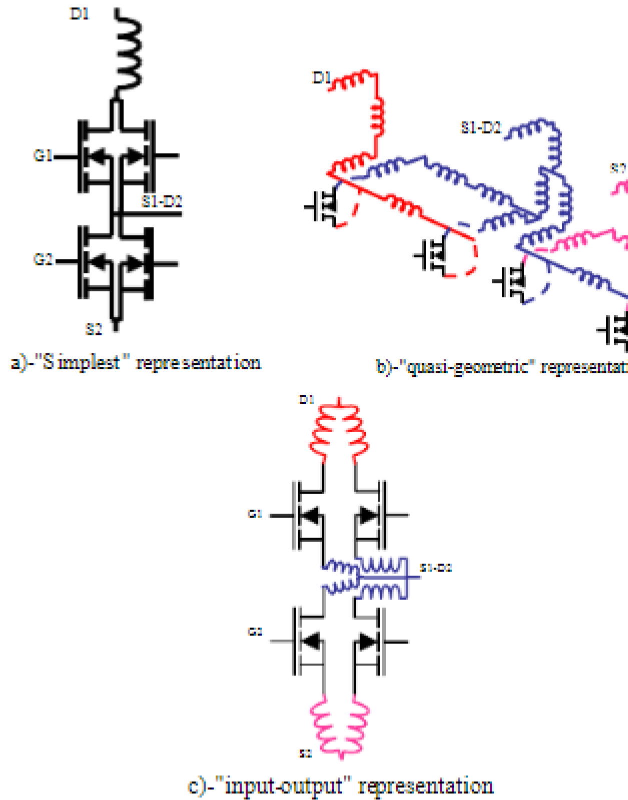

Figure 2. Different electrical equivalent circuits

Technology Development for Motor Drives (MD):

Fans, pumps and compressors used in many industrial, commercial and residential applications, offer significant opportunities for energy savings, since they are generally powered by constant-speed drives rather than by more energy-efficient adjustable-speed drives. For example, heating, ventilation, and air conditioning (HVAC) systems consume more than 20% of the total energy in the world, according to an EPRI report. Projections indicate that replacing constant-speed drives in current HVAC systems with adjustable-speed drives could save 35% of this energy. Although the benefits of adjustable speed control for many industrial, commercial and residential applications have been well documented, their success in large-scale production has been limited due to their higher purchase cost and perceived reliability limitations. However, effective means of integrating motor drives via the IPEM concept can achieve major improvements in cost, reliability, and performance. The major technology developments for motor drives are focused on active gate drivers to control dv/dt and di/dt, motor drive IPEM implementation to help reduce cost, and the use of double-sided cooling to improve thermal management of the motor drive IPEM.

RESULTS AND DISCUSIONS:

In today's world, power electronic conversion units have been used to transfer billions of kilowatts of electrical energy, especially within renewable energy systems. They are essential for the contribution of remarkable energy saving and environmental pollution control in broader perspective. European countries commit themselves that 20% of the entire electricity consumption will be provided through wind energy by 2020.

On the other hand, the increase in the energy estimated from renewable sources will lead even greater currents passing through the power electronic components; hence in future trends, the ability of withstanding the imposed stresses will be important factors in power

electronics module reliability. With this particular study, thermal management will be assessed for the power conversion elements of wind turbine system. More control among these devices, in terms of reliability, surely will bring more trust to wind energy systems and this would increase the number of national or locally owned businesses and investments. The presented work is essential for reliability of wind energy applications. The verification test of models showed very good agreement with the thermal profile supplied in the manufacturer's datasheet and could also be improved with experimental validation tests in future work.

CONCLUSION:

Advancements in semiconductor technologies have been the major driving force for improving converter size, weight, and cost; mostly due to increase in switching frequency. However, for some high frequency applications, fundamental limits in packaging are being reached. An order of magnitude increase in switching frequency will require substantial reduction in structural inductances associated with device and system-level packaging. Therefore, to provide further improvements in performance, reliability, and cost, it is essential to develop novel integration and packaging technologies in the form of Integrated Power Electronics Modules (IPEMs), which must enable the integration of all the converter functions and not only concentrate on the switching stage. These novel integration and packaging technologies, in conjunction with suitable devices, sensors and integrated design tools used to exploit the physical properties of available materials have been the focus of the CPES research program. The role of the technologies mentioned above in the IPEM concept is key to achieving high levels of integration and to enable significant growth of the power electronics industry. While technology roadblocks have been found to date, it is evident that further innovations will be necessary as power densities increase. The impacts of systems integration via IPEMs will enable a rapid growth of power electronics applications with reduced costs and design cycles that can be compared to the impacts in computer applications brought up by the VLSI circuit technology.

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