PRE-ENCODED MULTIPLIER BASED ON NON-REDUNDANT RADIX-4 SIGNED DIGIT ENCODING

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ABSTRACT

Multiplier is a simple component for implementing computationally intensive applications. Multimedia and virtual sign processing (DSP) packages (e.g., speedy Fourier remodel (FFT), audio/video formats) perform a large wide variety of multiplications with coefficients that do not change in the course of the execution of the utility. The research sports in the field of arithmetic optimization have proven that the layout of arithmetic components combining operations which proportion statistics, can cause large performance improvements. Modified booth (MB) encoding tackles the aforementioned limitations and reduces to half of the variety of partial products resulting to decreased location, vital postpone and power consumption. But, a committed encoding circuit is required and the partial products technology is extra complicated. A Non-Redundant radix-four Signed-Digit (NR4SD) encoding scheme extending the serial encoding technique. The proposed NR4SD encoding scheme uses one of the following sets of digit values: {-1,0,+1,+2}or{-2,-1,0,+1}. so one can cowl the dynamic variety of the two's complement form, all digits of the proposed representation are encoded according to NR4SD except the most vast one that is MB encoded. In this paper, we introduce structure of pre encoded multipliers for virtual sign Processing programs based totally on off line encoding of coefficients.

INTRODUCTION

VLSI layout provides papers in VLSI design, pc-aided layout, design evaluation, layout implementation, simulation and checking out. Its scope additionally consists of papers that cope with technical trends, pressing issues, and educational components in VLSI design

.The journal gives a dynamic international discussion board for authentic papers and tutorials through instructional, industrial, and different scholarly participants in VLSI design.

The development today's microelectronics spans a time which is even lesser than the common lifestyles expectancy modern-day a human, and yet it has visible as many as four generations. Early 60's saw the low density fabrication approaches classified beneath Small Scale Integration (SSI) in which transistor be counted changed into limited to approximately 10. This swiftly gave way to Medium Scale Integration inside the past due 60's when around 100 transistors might be located on a single chip.

It was the time when the value modern studies began to say no and private companies started out entering the competition in assessment to the earlier years in which the main burden became borne by using the army. Transistor-Transistor logic (TTL) offering better integration densities outlasted different IC households like ECL and have become the idea trendy the primary incorporated circuit revolution. It turned into the production modern day this latest that gave impetus to semiconductor giants like Texas instruments, Fairchild and national Semiconductors. Early 1970s marked the increase latest transistor matter to about

1000 per chip called the huge Scale Integration.

DESIGN OF VLSI

The complexity of VLSI is being designed and used today, which makes the manual approach to be impractical. Design automation is the order of the day. With the rapid technological developments in the last two decades, the status of VLSI technology is characterized by the following

1. A steady increase in the size and hence the functionality of the ICs.
2. A steady reduction in feature size and hence increase in the speed of operation as well as gate or transistor density.
3. A steady improvement in the predictability of circuit behaviour.
4. A steady increase in the variety and size of software tools for VLSI design.

ASIC DESIGN FLOW

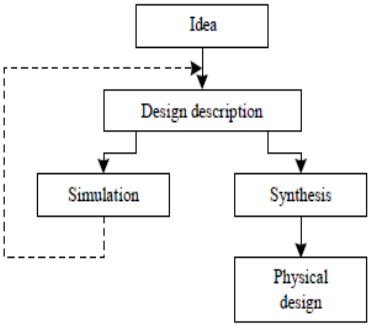
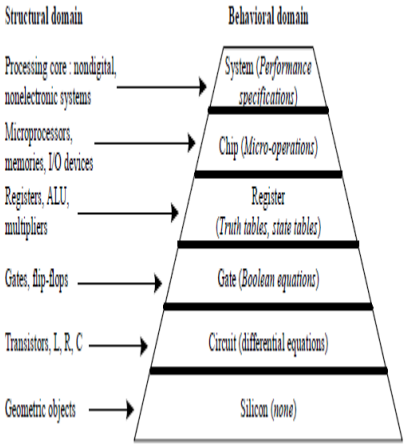


Fig 1.7 (a):Design flow of IC



ASIC DESIGN FLOW EXISTING PROJECT

Modified Booth is a redundant radix-4 encoding technique.Considering the multiplication of the 2's complement numbers A, B, each one consisting of n = 2k bits, B can be represented in MBform as:$B = (b_{n-1}\ldots\ldots b_0)_{2's} = -b_{2k-1}2^{2k-1} + \sum_{i=0}^{2K-2} b^i 2^i$

$= (b_{k-1}{}^{MB}\ldots\ldots b_0{}^{MB})_{MB} = \sum_{j=0}^{K-1} b^{MB} 2^{2j}$

Digits $b^{MB} \in \{-2, -1, 0, +1, +2\}$, $0 \le j \le k-1$, are formed asfollows:

$$b^{MB}_j = -2b_{2j+1} + b_{2j} + b_{2j-1}$$

Where $b_{-1} = 0$. Each MB digit is represented by the bits s, one and two. The bit s shows if the digit is negative (s = 1) orpositive (s = 0). One shows if the absolute value of a digit equals 1(one = 1) or not (one = 0). Two shows if the absolute value of a digitequals 2 (two = 1) or not (two = 0). Using these bits, we calculate theMB digits b^{MB}_j as follows:

$$b^{MB}_j = (-1)^{sj} .(onej + 2twoj)$$

Equations (4) form the MB encoding signals.

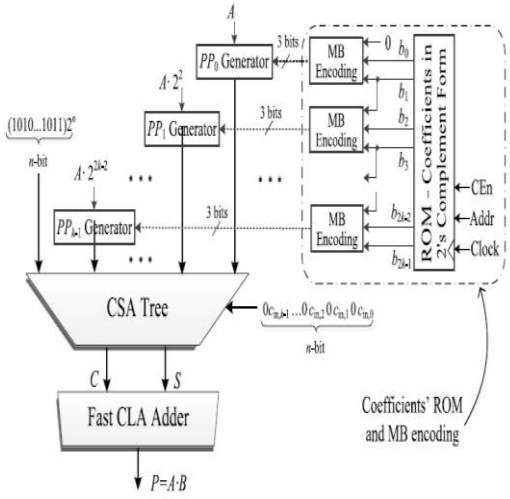
Sj= b2j+1, onej = b2j-1 ^ b2j;

twoj = (b2j+1 ^ b2j) ^ (~onej);

b_{2j+1}	b_{2j}	b_{2j-1}	b_j^{MB}	s_j	one_j	two_j
0	0	0	0	0	0	0
0	0	1	+1	0	1	0
0	1	0	+1	0	1	0
0	1	1	+2	0	0	1
1	0	0	−2	1	0	1
1	0	1	−1	1	1	0
1	1	0	−1	1	1	0
1	1	1	0	1	0	0

Modified Booth Encoding

The architecture of the system comprises the conventional MB multiplier and the ROM with coefficients in 2's complement form. Let us consider the multiplication A and B. The coefficient B = $(b_{n-1}\ldots\ldots b_0)_{2's}$ consists of n = 2k bits and is driven to the MB encoding blocks from a ROM where it is stored in 2's complement form. It is encoded according to the MB algorithm and multiplied by A= $(a_{n-1}\ldots\ldots a_0)_{2's}$, which is in 2's complement representation. We note that the ROM data bus width equals the width of coefficient B (n bits) and that it outputs one coefficient on each clock cycle.

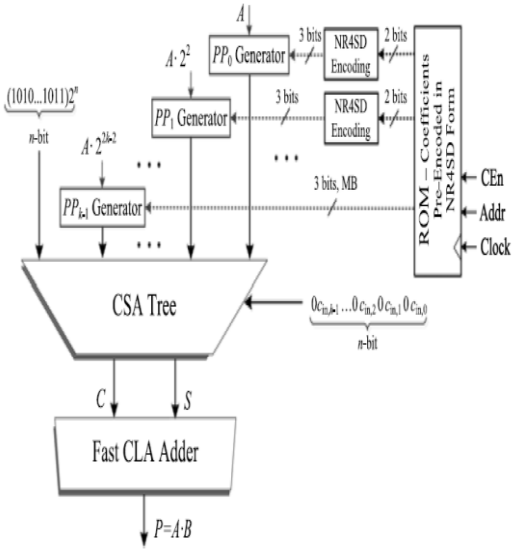


system architecture of the conventionalMB multipliers Modified Booth is a redundant radix-4 encoding technique. Each MB digit is represented by the bits s, one and two. The bit s shows if the digit is negative (s = 1) or positive (s = 0). One shows if the absolute value of a digit equals 1 (one = 1) or not (one = 0). Two shows if the absolute value of a digit equals 2 (two = 1) or not (two = 0).

PROPOSED PROJECT

A Non-Redundant radix-4 Signed-Digit (NR4SD) encoding scheme extending the serial encodingtechniques. The proposed NR4SD encoding schemeuses one of the following sets of digit values{-1,0,+1,+2} or {-2,-1,0,+1}. In order to cover the dynamic range of the 2'scomplement form, all digits of the proposed representation areencoded according to NR4SD except the most significant one thatis MB encoded.

BLOCK DIAGRAM



system architecture of the NR4SD multipliers the usage of the proposed encoding system, we pre-encode the standard coefficients and save them right into a ROM in a condensed shape (i.e., 2 bits in keeping with digit). as compared to the pre-encoded MB multiplier wherein the encoded coefficients need three bits in line with

digit, the proposed NR4SD scheme reduces the memory length. also, as compared to the MB form, which makes use of five digit values {-2, -1, zero, +1, +2} the proposed NR4SD encoding makes use of 4 digit values. as a consequence, the NR4SD based totally pre-encoded multipliers include a less complicated partial products era circuit. We discover the efficiency of the aforementioned pre-encoded multipliers contemplating the dimensions of the coefficients' ROM. the size of ROM used to shop the companies of coefficients is substantially decreased as well as the area and strength consumption of the circuit.

NR4SD^{+} Algorithm:

Step1. Consider the initial values j= 0 and c_0= 0.

Step2. Calculate the positively signed carry c_{2j+1} (+) and the negatively signed sum n^{-}_{2j} (-) of a HA* with inputs b_{2j} (+) and c_{2j} (+). The carry c_{2j+1} and the sum n_{-2j} of the HA* relate to its inputs as follows:

$$2c_{2j+1} - n^{-}_{2j} = b_{2j} + c_{2j}$$

The outputs of the HA* are analyzed at gate level in the following equations:

$$c_{2j+1} = b2j \mid c_{2j},\ n^{-}_{2j} = b_{2j} \wedge c_{2j}:$$

Step3. Calculate the carry c_{2j+2} and the sum n^{+}_{2j+1} of a HA with inputs b_{2j+1} and c_{2j+1}.

$$c_{2j+2} = b_{2j+1} \,\&\, c_{2j+1};\ n_{2j+1} = b_{2j+1} \wedge c_{2j+1}$$

Step4. Calculate the value of the b^{NR+}_{j} digit.

$$b^{NR+}_{j} = 2n^{+}_{2j+1} - n^{-}_{2j}$$

This result from the fact that n^{+}_{2j+1} is positively signed andn_{-2j} is negatively signed.

Step5. j = j + 1.

Step6. If (j < k- 1), go to Step 2. If (j = k - 1), encode the most significant digit according to MB algorithm and considering the three consecutive bits to be b_{2k-1}, b_{2k-2} and c_{2k-2} . If (j =k),stop.

$$one^{+}_{j} = n^{+}_{2j+1} \wedge n^{-}_{2j};$$
$$one^{-}_{j} = (\sim n^{+}_{2j+1}) \wedge n^{-}_{2j};$$
$$two^{+}_{j} = n^{+}_{2j+1} \wedge n^{-}_{2j}:$$

The minimum and maximum limits of the dynamic range in theNR4SD^{+} form are $-2^{n-1} - 2^{n-4} - 2^{n-6} - \ldots -1 < -2^{n-1}$ and$2^{n-1} + 2^{n-3} + 2^{n-5} + \ldots +2 < 2^{n-1}-1$. As observed in theNR4SD- encoding technique, the NR4SD+ form has larger dynamic range than the 2's complement form.Considering the 8-bit 2's complement number N, Table 4exposes the limit values -28 =-128, 28 - 1 = 127, and two typical values of N, and presents the MB, NR4SD^{-} and NR4SD^{+} digitsthat result when applying the corresponding encoding techniques to each value of N we considered. We added a bar above the negatively signed digits in order to distinguish them from the positively signed ones.

RESULTS

RTL SCHEMATIC (SYNTHESIS)

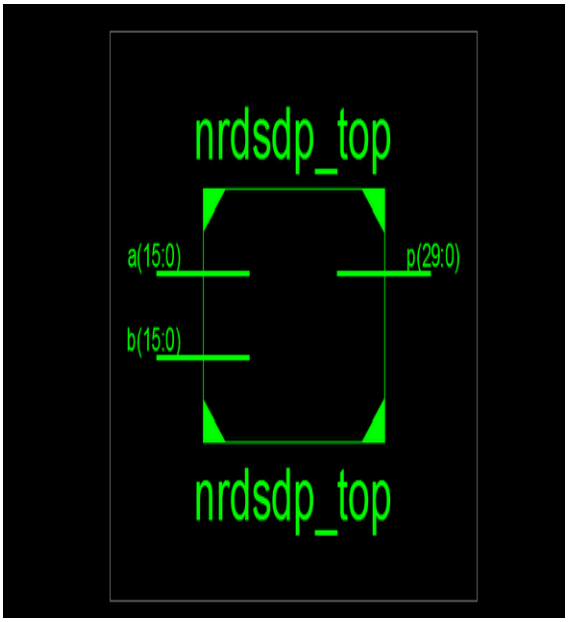


Fig 6.1: Top module of Multiplier

6.2: RTL Schematic of Multiplier

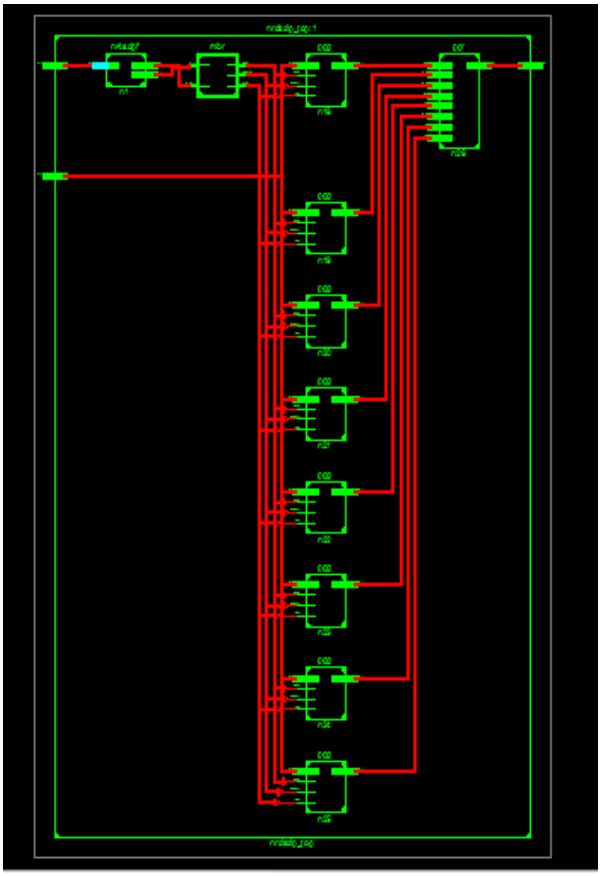


Fig 6.2: RTL Schematic of Multiplier

FUTURE SCOPE

This method can also be implemented for 32 bit, 64 bit and 124 bit.Pre -encoded NR4SD multipliers are used to perform arithmetic operations in advanced microprocessors and microcontrollers with more speed and less power consumption than the Modified Booth scheme

.CONCLUSION

a new layout of pre-encoded multipliers is explored by means of off-line encoding the usual coefficients and storing them in machine reminiscence. We propose encoding those coefficients within the Non-Redundant radix-four Signed-Digit (NR4SD) shape. The proposed Pre-encoded NR4SD multiplier designs are more region and electricity green compared to the conventional and pre-encoded MB designs. Synthesis and Simulation evaluation in Xilinx 14.five software the usage of Verilog hardware Description Language verifies the gains of the proposed pre-encoded NR4SD multipliers in phrases of area complexity and strength intake as compared to the traditional MB multiplier.

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