SMART GRID APPLICATION FOR BIDIRECTIONAL INTELLIGENT SEMICONDUCTOR TRANSFORMER

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Abstract

This paper proposes a brand new bidirectional intelligent semiconductor transformer (BIST) for the clever distribution sys-tem and clever grid. The proposed BIST consists of excessive-voltage high-frequency ac/dc converter, bidirectional low-voltage dc/dc converter, and hybrid-switching dc/ac inverter. It functions 1) input-to-output isolation with a high-frequency transformer; 2) bidirec-tional electricity flow; three) small size and light weight; four) capability of compensating voltage sag and/or swell; and five) cognizance of 3-section structure primarily based on single-section module. The opera-tional feasibility of proposed transformer became verified no longer only with the aid of pc simulation with PSCAD/EMTDC software program however additionally by a hardware prototype with rating of 1.9 kV/127 V, 2 kVA, allowing a 3-section transformer of 3.3 kV/220 V, 6 kVA with 3-segment creation

Key Words: *PSCAD, EMTDC, transformer*

INTRODUCTION

conventional transformer composed of coil and iron center can exchange best the importance of the ac voltageand the high-quality of providing power is absolutely dependent on that of the enter strength. Sensible semiconductor transformer or solid-state transformer was proposed by using EPRI to replace the traditional transformer in railway structures and substations, wherein light weight is mandatorily required. Currently, EPRI has mentioned a hundred kVA unmarried-section semiconductor transformer named clever universal transformer for distribution automation.

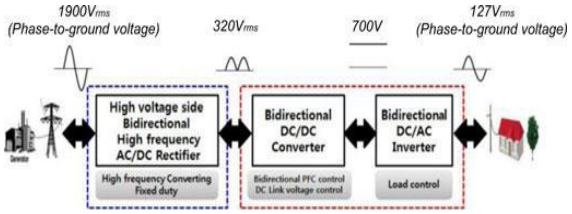
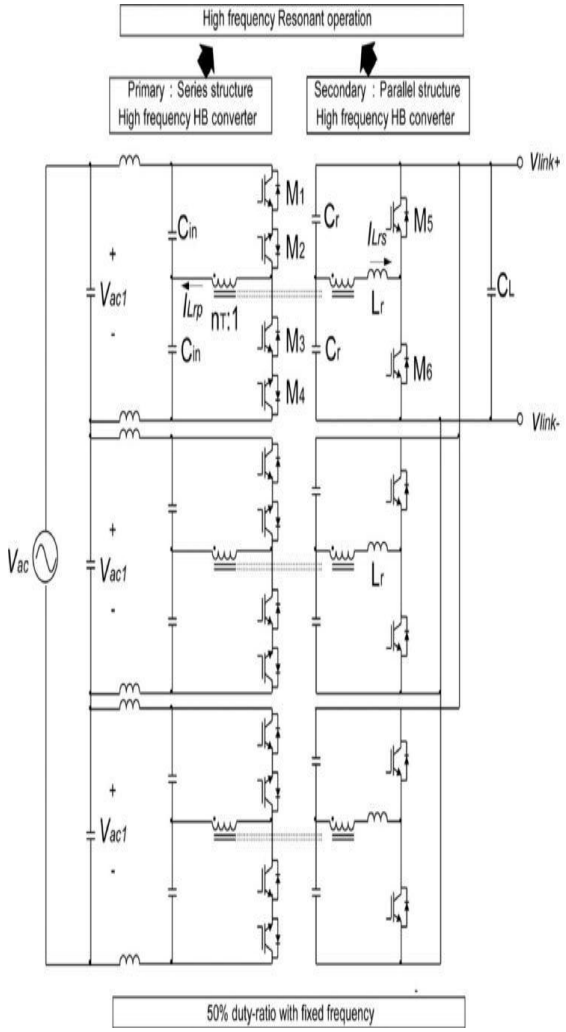


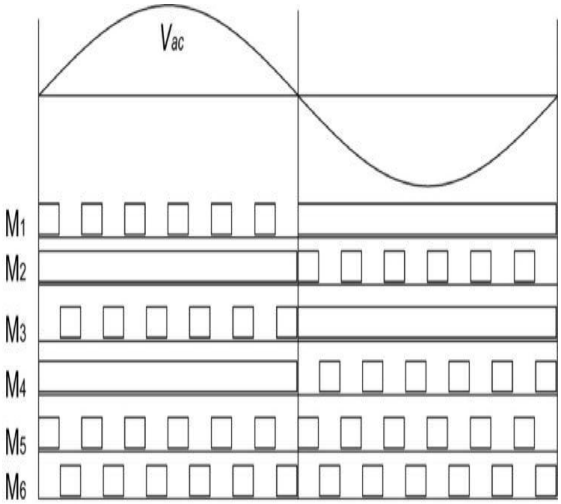
Fig:Configuration of the BIST.

power, however also 86f68e4d402306ad3cd330d005134dac ac energy to the client by way of com-pensating the voltage sag, swell, and harmonics So, it could be utilized for enforcing the smart distribution machine and the microgrid. diverse styles of clever semiconductor transformers were already proposed. but, for the reason that strength drift in those transformers is unidirectional, it is not nicely ap-plicable for the dc distribution and microgrid. you'll find a few studies at the semiconductor transformer topologies with bidirectional electricity float functionality. In bidirectional power go with the flow can be accomplished but the electricity issue isn't always controlled. The topology in can compensate sag/swell voltage; but, it employs heavy and cumbersome line-frequency transformer for isolation. The semi-conductor transformer in has now not only the bidirectional electricity flow features but additionally voltage sag repayment in which excessive-frequency dc/dc power conversion is employed. The circuit configuration in, however, shows too many active switch-ing device counts, as a minimum 18 IGBTs for imposing

single-phase module. In, 3-level shape constituted of ac/dc converter, dual-energetic-bridge dc/dc converter, and inverter. these topologies provide energy factor correction and reactive electricity reimbursement, however they be afflicted by heavy turn-off loss in dc/dc stage and complex manage for voltage balancing.

This paper proposes a brand new bidirectional shrewd semicon-ductor transformer (BIST) for the clever distribution gadget and microgrid. The proposed BIST includes high-voltage part and occasional-voltage element, whose configuration is proven in Fig. 1. The excessive-voltage component is composed of numerous 1/2-bridge ac/dc converters linked in collection via excessive-frequency trans-formers to cope with high enter voltage, while the low-voltage element consists of bidirectional half of-bridge dc/dc converter and dc/ac PWM inverter. in the prototype BIST, the input volt-age on the high-voltage aspect is 1900 V and the output voltage at the low-voltage facet is 127 V, in which the number one and sec-ondary dc-hyperlink voltages are 320 V and seven hundred V, respectively. A three-segment 3.3 kV/220 V transformer may be constructed the usage of three gadgets of one.9 kV/127 V single-section module.





II. PROPOSED SEMICONDUCTOR TRANSFORMER

A. High-Voltage Part

Fig. 2 indicates the energy circuit of ac/dc rectifier, which con-verts unmarried-phase ac voltage of 1900 V into full-bridge-rectified waveform of 320 V. The ac/dc converter has excessive-frequency transformers, which offer excessive-frequency resonance and enter– output isolation. The input facet works below high voltage, while the output side works underneath low voltage. So, the input aspect is designed with 3 half-bridge modules related in collection, wherein IGBT gadgets are linked in collection in the reverse path. The output aspect is designed with 3 1/2-bridge modules linked in shunt. complete device operates in bidirec-tional excessive-frequency resonance mode underneath a hard and fast frequency with 50% duty ratio to lessen system size and switching loss. due to the fact the resonant degree is largely an LLC converter, the enter-to-output benefit of every resonant converter, that is described through vlin k/|va c 1|, is determined only by its transformer turns-ratio nTif the resonant frequencyfris identical to the switching fre-quencyfsr [24], where va c 1 is the input voltage of each resonant degree and it's miles identical to va c /3. since the enter and output filter capacitors of Cin and CL are a lot larger than Cr and para-sitic capacitances of switches are much smaller than Cr , the resonant frequency fr , which is same to fsr , is calculated as 1/[2π(2LrCr)0.5] with resonant inductor Lr and resonant capacitors of Cr . Fig. 3 indicates the switching pulses for each switch in a unmarried-module of the bidirectional excessive-frequency ac/dc converter in keeping with the polarity of the ac enter volt-age. The gating pulses for each switch are generated with equal pattern irrespective of the path of strength glide. earlier than ex-planation, it's miles assumed that the magnetizing inductance Lm is infinity.

Mode 1: The direction of energy go with the flow is forward and thepolarity of input voltage is high quality as shown in Fig. 4(a). inside the first degree, the number one present day flows via the transistor in

M1and the diode in M2when M1turns ON. At this example,the secondary cutting-edge flows thru diode in M5 . within the next degree, the primary modern-day flows thru the transistor in M3 and the diode in M4 while M3 activates. At this example, the secondary modern-day flows thru the diode in M6 .

Mode 2: The course of strength go with the flow is forward and thepolarity of enter voltage is terrible as shown in Fig. four(b). within the first stage, the primary modern flows thru the transistor in M2and the diode in M1when M2turns ON. At this example,the secondary cutting-edge flows thru diode in M6 . in the subsequent degree, the primary cutting-edge flows through the transistor in M4 and the diode in M3 while M4 turns on. At this example, the secondary cutting-edge flows through the diode in M5 .

Mode 3: The path of power drift is backward and thepolarity of input voltage is effective as proven in Fig. 4(c). within the first stage, the secondary contemporary flows thru transistor in M5 whilst M5 turns on. At this instance, the number one contemporary flows thru the diode in M1 and the transistor in M2 . within the next degree, the secondary modern-day flows through the transistor in M6 when M6 activates. At this instance,

the primary modern flows via the diode in M3 and the transistor in M4 .

Mode 4: The direction of strength float is backward and thepolarity of enter voltage is negative as proven in Fig. 4(d). within the first level, the secondary present day flows through transistor in M6 when M6 turns on. At this example, the primary present day flows thru the transistor in M1 and the diode in M2 . in the subsequent level, the secondary cutting-edge flows through the transistor in M5 while M5 turns on. At this instance, the number one current flows via the transistor in M3 and the diode in M4 .

B. Low-Voltage part

The low-voltage component includes the dc/dc converter and the dc/ac inverter related in cascade as shown in Fig. 5. The dc/dc converter adjustments the total-bridge rectified waveform of 320 V into the constant dc voltage of seven hundred V and the dc/ac inverter changes the regular dc voltage of seven-hundred V into the single-segment ac voltage of 127 V. The dc/dc converter and dc/ac inverter use a hybrid transfer with IGBT and MOSFET linked in parallel. The dc/dc converter and dc/ac inverter are composed of 1/2-bridges related in cascade. The dc/dc converter operates to control the strength component and the dc-hyperlink voltage, even as the dc/ac inverter operates to control the output voltage. because the switching frequency in IGBT will increase, the switching loss will increase because of tail-current, which critically reduces the system efficiency. so that it will improve this switching loss, a MOSFET is hooked up in parallel to implement a hybrid switch. Fig. 6 shows a way to deliver the gating signal to the hybrid transfer. The MOSFET activates a few microseconds beforehand whilst the IGBT switch turns OFF. After the MOSFET activates, the IGBT turns OFF at once and the MOSFET turns OFF at the immediate that the IGBT is firstly to turn OFF. Hybrid switching gives reduction of recovery loss due to tail-contemporary. If a diode is connected in series with MOSFET, MOSFET destruction because of counter electromotive force can be blanketed. If resistance is attached in parallel with diode, ringing phenomenon can be decreased.

C. Zero-Voltage-Switching (ZVS) Operation

because the magnetizing inductance Lm can not have infinity value in real transformer, operational modes are particularly dif-ferent from that explained in Fig. four and it's miles helpful to acquire tender-switching of switches. All modes in Fig. 4 have identical ZVS operation so that operational mode analysis is explained based totally on mode 1 of ahead strength drift with tremendous input voltage. Fig. 7 shows ZVS operation in mode 1 whilst the magnetizing inductance isn't always infinity. before rationalization, it's miles assumed that the resonant frequency fr is identical to the switching frequency fsr.

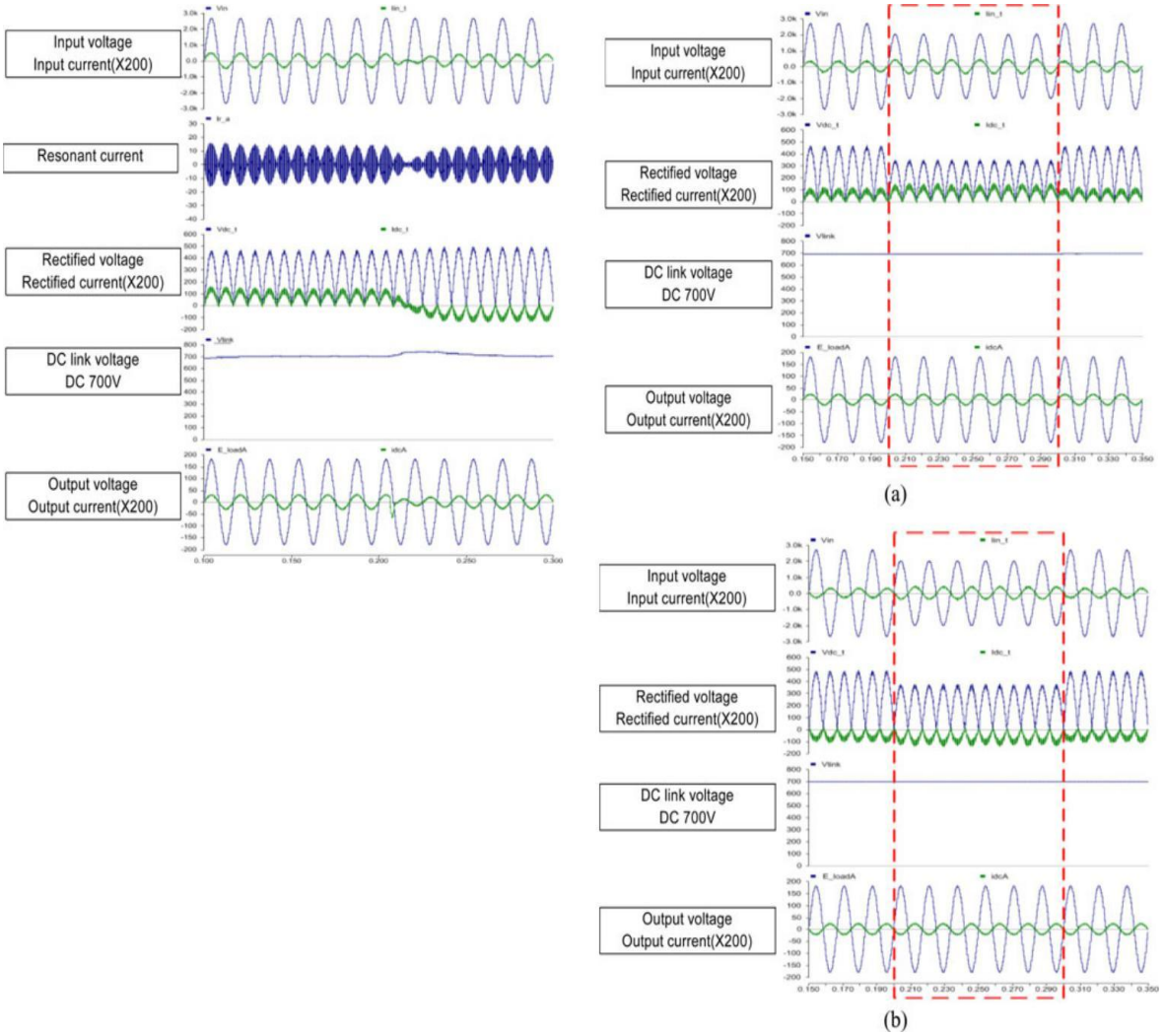
Mode A: The magnetizing modern prices collector–emittercapacitance of M3Cc e,M3 and discharges collector–emitter ca-pacitance of M1Cc e,M1 . for this reason, collector–emitter voltage of M3vce,M3increases and collector–emitter voltage of M1vce,M1decreases. while vce,M3 exceeds the source voltage or vce,M1 crosses 0, the frame diode of M1 starts offevolved to conduct the cutting-

edge. At this instant, the mode A starts off evolved. during mode A, the secondary resonant contemporary iL r s begins to waft with resonant manner and it's far divided into half of and each 1/2 currents drift thru the 2 resonant capacitors as shown in Fig. 7(a). The number one resonant present day iL r p is the sum of the magnetizing current iM and secondary resonant stated the primary side, which can be expressed as iL r s /nT . for the reason that iL r s /nT is smaller than iM , the number one resonant cutting-edge iL r p is poor so that it flows via frame diode in M1 and transistor in M2 from the negative height price of the magnetizing current—IM ,p ok . This mode keeps till iL r s /nT is identical to iM .

Mode B: AfteriL r s/nTis more thaniM,iL r pflows throughtransistor in M1 and body diode in M2 . because the resonant frequencyfr is identical to the switching frequency fsr, iL r s is almost decreased to 0 at the end of this mode.

Mode C: WhenM1is turned OFF, most effective the magnetizingcurrent remains on the number one aspect and it may be assumed that the magnetizing present day is steady due to the fact mode C is a short lifeless-time period. As shown in Fig. 7(c), all switches of M1and M3are in flip-off state in order that they may be modeledas their collector–emitter capacitances of Cc e,M1 and Cc e,M3 . consequently, the magnetizing contemporary flows through paths of Lm, Cin , collector–emitter capacitance of M1Cc e,M1 , frame diode in M2 and Lm, Cin , transistor in M4 , collector–emitter capacitance of M3Cc e,M3 . consequently, Cc e,M1 is charged from 0 to va c 1 by the 1/2 of the magnetizing modern-day and Cc e,M3 is discharged from va c 1 to zero with the aid of the half of the magnetizing current. If mode C operation is finished before M3 is became ON, ZVS of M3 can be executed. ZVS of M1 has the identical way as that of M3 . Fig. 8 is pc simulation of ZVS operation in mode 1 of ahead strength float with the superb input voltage. It indicates that the simulation waveforms are just like those shown in Fig. 9. D. Transformer Design

Fig. 9 is the operational waveform of the LLC resonance con-verter during half of the line cycle. To analyze the proposed



the 50-kHz resonant cutting-edge for ZVS when the power drift is reversed from forward to backward at zero.18 ms. The 0.33 graph suggests the output voltage waveform with the whole-bridge rectified voltage and modern. The fourth graph shows the dc-hyperlink volt-age, which maintains regular voltage of seven hundred V with negligible ripples. The fifth graph indicates the output voltage and modern, which are almost sinusoidal with negligible harmonics. through the simulation effects, it is showed that the proposed semi-conductor transformer operates well as analyzed with the theoretical method. Fig. eleven indicates simulation outcomes to test the operation of the proposed semiconductor transformer un-der enter voltage sag in ahead electricity glide and opposite power flow. Fig. eleven(a) shows the input voltage and present day, rectified voltage and modern-day, dc-hyperlink voltage, and output voltage and current when sag takes place inside the ahead energy flow. The in-put contemporary and rectified contemporary slightly growth for the duration of sag to keep same enter strength. The dc-link

voltage is maintained with seven-hundred V through the voltage control of the dc/dc converter. Fig. eleven(b) indicates the enter voltage and cutting-edge, rectified volt-age and current, dc-link voltage, and output voltage and current when sag takes place within the reverse energy go with the flow. The input cutting-edge and rectified contemporary slightly increase throughout sag to hold identical power. The dc-hyperlink voltage is maintained with seven hundred V thru the voltage control of dc/dc converter.

CONCLUSION:

in this paper, a new configuration of the BIST changed into proposed, which has rating of 1.nine kV/127 V, 2 kVA. The transformer includes the high-voltage excessive-frequency ac/dc rectifier, and low-voltage dc/dc and dc/ac converters. The operational fea-sibility of the proposed transformer was confirmed with the aid of laptop simulation with PSCAD/EMTDC software. primarily based at the simu-lation consequences, a hardware prototype with rating of 1.9 kV/127 V, 2 kVA turned into constructed and tested within the lab to verify the feasibility of hardware implementation. using 3 gadgets of this transformer, a 3-phase transformer with score of three.3 kV/220 V, 6 kVA may be built. The proposed transformer can be relevant for enforcing the smart grid.

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