A NOVEL STATCOM BASED ON PARALLEL-CONNECTED DIODE-CLAMPED MODULAR MULTILEVEL CONVERTERS

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ABSTRACT

A new static synchronous compensator (STAT- COM) based on the on the parallel connected diode clamped modular multilevel converter (parallel-DCM2C) is proposed in this paper. In this converter topology, the capacitor voltage is clamped by using a low power rating diode in each submodule. The quantity of voltage sensors is significantly reduced and is free from the number of voltage levels. Furthermore, the voltage balancing control method becomes very simple and the capacitor voltage balance speed is fast. Based on the structure of modular multilevel converter, the DCM2C-STATCOM has the capability of Var compensation and negative-sequence current compensation. The topology characteristics and compensation control method of parallel DCM2C-STATCOM are investigated in this paper.

1.0 INTRODUCTION

NOWADAYS, in medium-voltage distribution systems, many power quality issues, such as low power factor, harmonic distortion, and unbalanced voltage, are resulted from the unbalanced loads and nonlinear loads. To improve the power quality, the static synchronous compensators (STATCOM) are widely used on the grid side to achieve high power factor and low distortion. Recently, STATCOM based on multilevel converters are very popular in medium-voltage networks, including flying-capacitor multilevel converters (FCMC), diode-clamped multilevel converters (DCMC), and cascaded H-bridge multilevel converters (CHMC) [1]–[7]. Because there is a dc bus in the topology of the FCMC and DCMC, they have stronger capability of negative-sequence current compensation than the CHMC with star configuration and they can be used in the applications of ac/dc power conversion. However, the poor modularity and significantly increasing capacitors and power diodes restrict their applications in medium/high-voltage networks. The CHMC with star configuration has good modularity and is very popular in medium-voltage Var compensation applications. In , a hierarchical voltage balancing control method is carried out with the phase-shifted unipolar sine PWM method. Based on the same control structure, the low-voltage ride-through issue is solved in. But the CHMC with star configuration has very weak negative-sequence compensation capability. The CHMC with delta configuration can overcome that defect [13], but the voltage across the arm of the converter is line voltage and the number of submodules (SM) in an arm is increased a lot. Since it was applied in TransBay project in 2010, the modular multilevel converter (MMC) topology has gained growing attentions in many applications, such as high-voltage direct current transmission systems, flexible alternating current transmission systems, and STATCOM. The MMC topology is very promising in mitigation of all the power quality problems. The structure and operating principles for MMC-STATCOM in distorted and unbalanced grid have been widely researched. Mohammadi and

TavakoliBina proposed an MMC-STATCOM configuration used for medium-voltage large-current system and an extended configuration EMMC-STATCOM used for highpower applications in [18]. Du and Liu presented an MMCbased D-STATCOM system, which is able to compensate the seriously unbalanced nonlinear load while keeping all the floating capacitor voltages regulated [19]. Though the MMC topology has many advantages in Var compensation, the capacitor voltage balancing control for all the floating SMs in each leg remains to be a challenging issue, which is a common problem in most multilevel converters [22]–[28]. Usually, to realize the capacitor voltage balancing control, a large number of voltage sensors are needed and the amount of calculation in controllers is increased a lot, which maybe prolong the digital control cycle. With the converter voltage levels increasing, the situation will become worse. In [29], a kind of DCMC topology is proposed by using the clamping diodes to clamp the capacitor voltages of a multilevel converter with star configuration. The capacitor voltage balancing control is simplified a lot and the number of capacitor voltage sensors is reduced a lot. However, the negative-sequence current compensation capability is weak and an energy feedback circuit is required. In this paper, the diode-clamped modular multilevel converter (DCM2C) is developed. A balancing branch, which consists of a low power rating diode and an inductor, is added to each SM. With the help of the balancing branches, the capacitor voltages are clamped and sorted naturally from the bottom SM to the top SM in each arm, and the clamping current pulse can be suppressed. As a result, only the capacitor voltage of the top SM or the bottom SM needs to be measured in each arm. With a simple voltage control method, the capacitor voltage of the top or bottom SM can be controlled to the reference value and then all the SM capacitor voltages in this arm can be balanced. Although the clamping diodes and inductors are required in the DCM2C topology, the reducing cost of voltage sensors and the simplifying of capacitor voltage balancing control have great significance. In this paper, the power circuit and control algorithm of the DCM2C-STATCOM are discussed in detail.

PROPOSED CONVERTER DESIGN&OPERATION

PROPOSED CIRCUIT

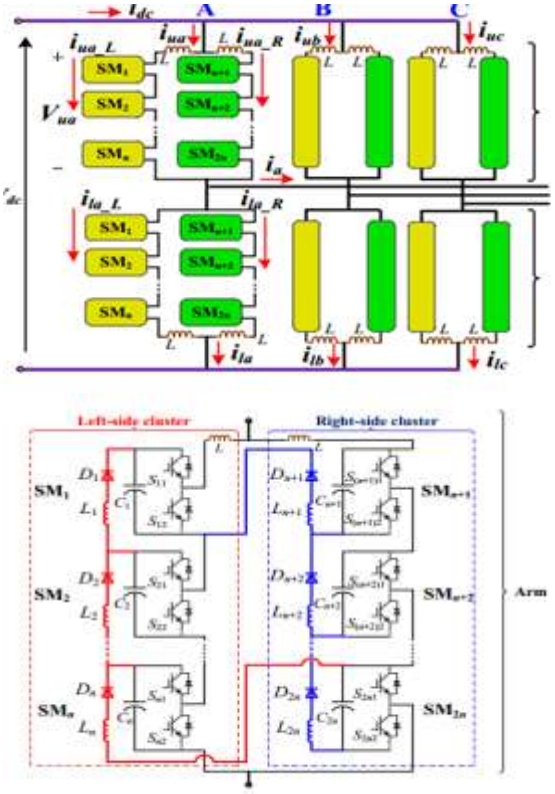


Fig 2 Topology of the parallel-DCM2C. (a) Three phase structure; (b) One arm structure.

STRUCTURE OF DCM2C-STATCOM

Based on the traditional MMC, the structure of STATCOM configuration is shown in Fig. 5.1. On the grid side, Vsj (j = a, b, c) are the voltage sources. The unbalanced and nonlinear load, for example, the single-phase ac traction system, causes power quality issues, which are expected to be solved by STATCOM.

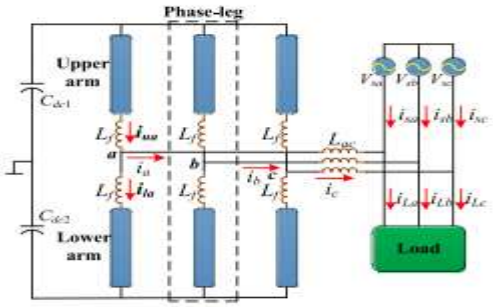


Fig5. 1. MMC-STATCOM circuit configuration

On the converter side, each phase leg consists of an upper arm, a lower arm, and two arm inductors. Bulk capacitors are connected to the dc link. The STATCOM connects to the grid through the ac inductors Lac. As shown in Fig 5.2, each arm contains n SMs, denoted as SM1−SMn.

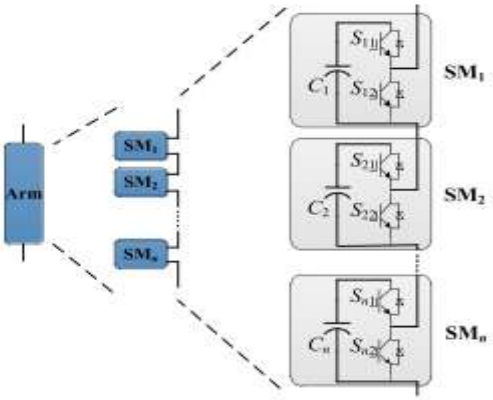


Fig 5.2 Structure of SMs in MMC topology.

A typical SM consists of a dc energy storage capacitor and two power switches (e.g., IGBT). The topology proposed in [29] uses clamping diodes to sort the SM capacitor voltages in one phase arm and the diodes have a good performance in the balancing process of the capacitor voltages, as shown in Fig.5.3(a).

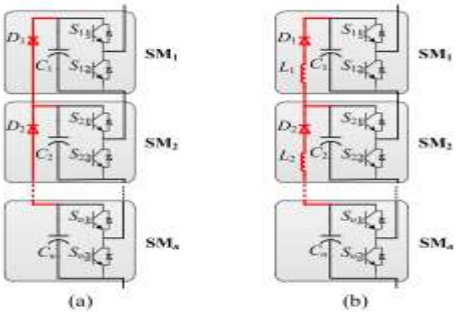
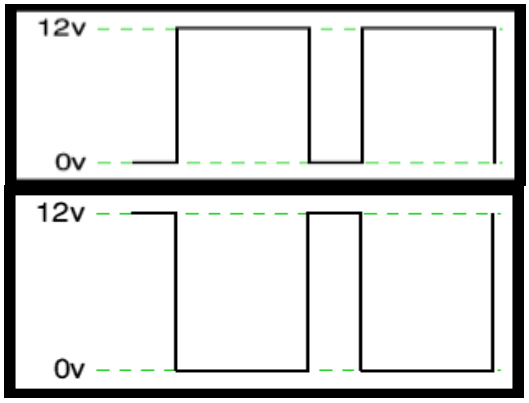


Fig5. 3. Connection diagrams of SMs with balancing branches. (a) Using diodes to clamp capacitor voltages. (b) Using diodes and inductors to clamp capacitor voltages

The converter runs very well in the steady state; however, there is a potential problem when a high voltage deviation exists between two neighboring SM capacitors in the abnormal conditions. For example, in the starting process of the converter, the current flowing through the clamping diode will be of high pulses, which may damage the switches. In addition, the current rating of the clamping diodes should be high enough for the recovery from severe unbalance conditions. Fig.5. 3(b) shows an improved topology. A buffer inductor connected to the clamping diode in serial is used to suppress the current pulses. Considering that the basic structure of the proposed converter is the MMC; this converter is called the diode-clamped MMC. For simplicity, all the devices in the DCM2C are assumed to be ideal devices. Fig. 5.4(a) shows the connection diagram of two neighboring SMs in each arm of DCM2C. In this paper, the phase-shifted carrier pulse width modulation (PSC-PWM) method is employed. According to the principles of PSC-PWM, there is a phase shift θ between the each two neighboring triangle carrier waves.

PULSE WIDTH MODULATION

Pulse Width Modulation (PWM) is the most effective means to achieve constant voltage battery charging by switching the solar system controller's power devices. When in PWM regulation, the current from the solar array tapers according to the battery's condition and recharging needs Consider a waveform such as this: it is a voltage switching between 0v and 12v. It is fairly obvious that, since the voltage is at 12v for exactly as long as it is at 0v, then a 'suitable device' connected to its output will see the average voltage and think it is being fed 6v - exactly half of 12v.



By varying - or 'modulating' - the time that the output is at 12v (i.e. the width of the positive pulse) we can alter the average voltage. So we are doing 'pulse width modulation'. I said earlier that the output had to feed 'a suitable device'. A radio would not work from this: the radio would see 12v then 0v, and would probably not work properly. However a device such as a motor will respond to the average, so PWM is a natural for motor control.

Pulse Width modulator

So, how do we generate a PWM waveform? It's actually very easy, there are circuits available in the TEC site. First you generate a triangle waveform as shown in the diagram below. You compare this with a d.c voltage, which you adjust to control the ratio of on to off time that you require. When the triangle is above the 'demand' voltage, the output goes high. Half the time the output is high and half the time it is low. Fortunately, there is an IC (Integrated circuit) called a comparator: these come usually 4 sections in a single package. One can be used as the oscillator to produce the triangular waveform and another to do the comparing, so a complete oscillator and modulator can be done with half an IC and maybe 7 other bits.

The triangle waveform, which has approximately equal rise and fall slopes, is one of the commonest used, but you can use a saw tooth (where the voltage falls quickly and rinses slowly). You could use other waveforms and the exact linearity (how good the rise and fall are) is not too important.

Space Vector PWM

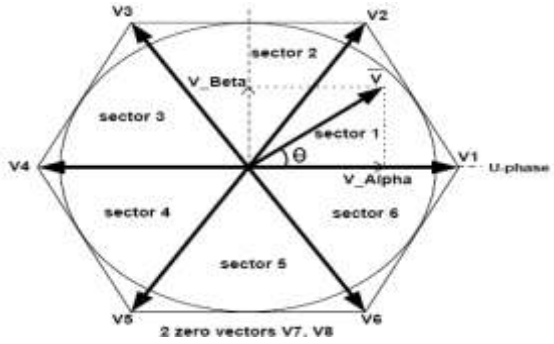
The Space Vector PWM generation module accepts modulation index commands and generates the appropriate gate drive waveforms for each PWM cycle. This section describes the operation and configuration of the SVPWM module.

The inverter fundamental line-to-line Rms output voltage (Vline) can be approximated (linear range) by the following equation:

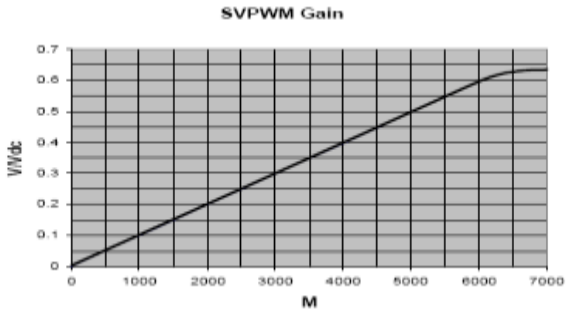
$$Vline = Umag * Mod\_Scl * Vdc / \sqrt{6} / 2^{25}$$

…….. (1)

Where dc bus voltage (Vdc) is in volts



Space Vector Diagram



Transfer Characteristics

The maximum achievable modulation (Umag_L) in the linear operating range is given by:

$$Umag\_L = 2^{25} * \sqrt{3} / Mod\_Scl$$

…

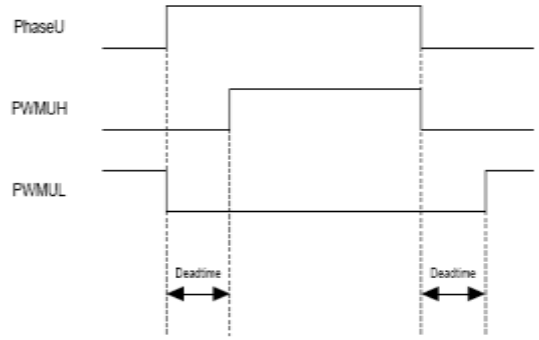
…Over modulation occurs when modulation Umag > Umag_L.

PWM Operation

Upon receiving the modulation index commands (UAlpha and UBeta) the sub-module SVPW M_Tm starts its calculations at the rising edge of the PWM Load signal. The SVPWM _Tm module implements an algorithm that selects (based on sector determination) the active space vectors (V1 to V6) being used and

calculates the appropriate time duration (w.r.t. one PWM cycle) for each active vector. The appropriated zero vectors are also being selected. The SVPWM _Tm module consumes 11 clock cycles typically and 35 clock cycles (worst case Tr) in over modulation cases. At the falling edge of nSYNC, a new set of Space Vector times and vectors are readily available for actual PWM generation (PhaseU, PhaseV, PhaseW) by sub module Pwm Generation. It is crucial to trigger PwmLoad at least 35 clock cycles prior to the falling edge of nSYNC signal; otherwise new modulation commands will not be implemented at the earliest PWM cycle.

The dead time insertion logic chops off the high side commanded volt*seconds by the amount of dead time and adds the same amount of volt*seconds to the low side signal. Thus, it eliminates the complete high side turn on pulse if the commanded volt*seconds is less than the programmed dead time.

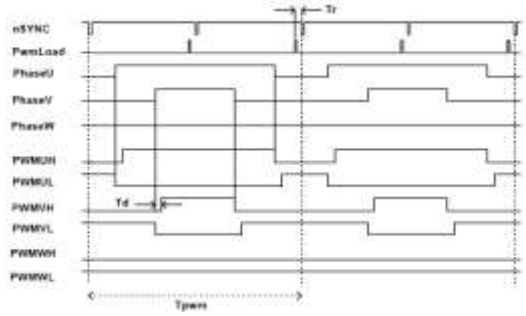


Dead time Insertion

The dead time insertion logic inserts the programmed dead time between two high and low side of the gate signals within a phase. The dead time register is also double buffered to allow "on the fly" dead time change and control while PWM logic is inactive.

Symmetrical and Asymmetrical Mode Operation

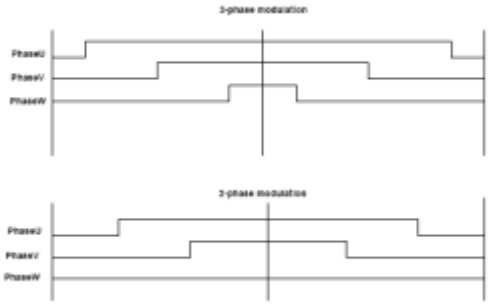
There are two modes of operation available for PWM waveform generation, namely the Center Aligned Symmetrical PWM (Figure) and the Center Aligned Asymmetrical PWM (Figure)The volt-sec can be changed every half a PWM cycle (Tpwm) since Pwm Load occurs every half a PWM cycle (compare Figure :symmetrical pwm and Figure :asymmetrical PWM). With Symmetrical PWM mode, the inverter voltage Config = 0), the inverter voltage can be changed at two times the rate of the switching frequency. This will provide an increase in voltage control bandwidth, however, at the expense of increased current harmonic



Asymmetrical PWM Mode

Three-Phase and Two-Phase Modulation

Three-phase and two-phase Space Vector PWM modulation options are provided for the IRMCx203. The Volt-sec generated by the two PWM strategies are identical; however with 2-phase modulation the switching losses can be reduced significantly, especially when high switching frequency (>10Khz) is employed. Figure: three-phase and two phase modulation shows the switching pattern for one PWM cycle when the voltage vector is inside sector 1

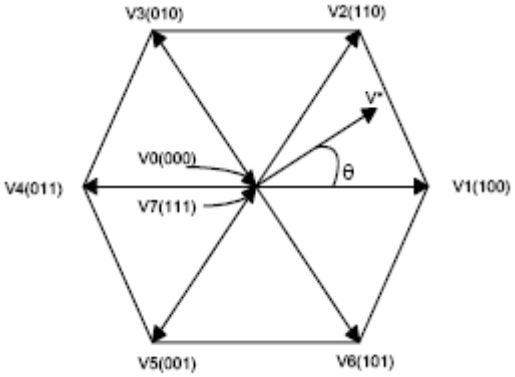


Sinusoidal Pulse Width Modulation

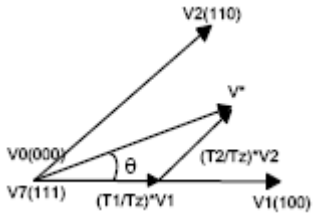
In many industrial applications, Sinusoidal Pulse Width Modulation (SPWM), also called Sine coded Pulse Width Modulation, is used to control the inverter output voltage. SPWM maintains good performance of the drive in the entire range of operation between zero and 78 percent of the value that would be reached by square-wave operation. If the modulation index exceeds this value, linear relationship between modulation index and

output voltage is not maintained and the over-modulation methods are required

space vector shows 8 space vectors in according to 8 switching positions of inverter, V* is the phase-to-center voltage which is obtained by proper selection of adjacent vectors V1 and V2.



Inverter output voltage space vector

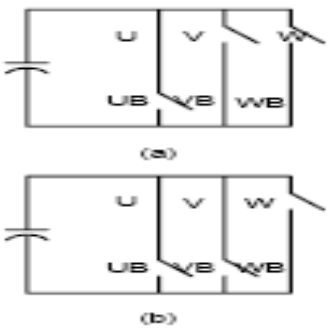


Determination of Switching times

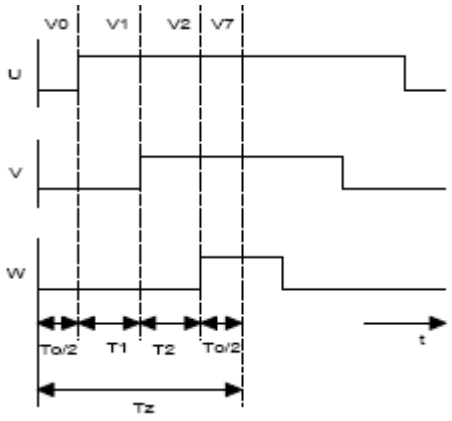
The reference space vector V* is given by Equation (1), where T1, T2 are the intervals of application of vector V1 and V2 respectively, and zero vectors V0 and V7 are selected for T0.

$$V^* T_z = V1 *T1 + V2 *T2 + V0 *(T0/2) + V7 *(T0/2) \quad \ldots\ldots\ldots (4)$$

Fig. below shows that the inverter switching state for the period T1 for vector V1 and for vector V2, resulting switching patterns of each phase of inverter are shown in Fig. pulse pattern of space vector PWM.



Inverter switching state for (a)V1, (b) V2



Pulse pattern of Space vector PWM

Comparison

In Fig:- comparison, U is the phase to- center voltage containing the triple order harmonics that are generated by space vector PWM, and U1 is the sinusoidal reference voltage. But the triple order harmonics are not appeared in the phase-to-phase voltage as well. This leads to the higher modulation index compared to the SPWM.

Comparison of SPWM and Space Vector PWM

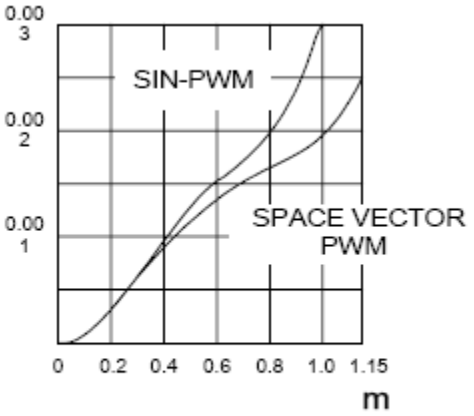
As mentioned above, SPWM only reaches to 78 percent of square wave operation, but the amplitude of maximum possible voltage is 90 percent of square-wave in the case of space vector PWM. The maximum phase-to-center voltage by sinusoidal and space vector

PWM are respectively

$V_{max} = V_{dc}/2$: Sinusoidal PWM

$V_{max} = V_{dc}/\sqrt{3}$: Space Vector PWM

Where, Vdc is DC-Link voltage.



(a)rms harmonic current

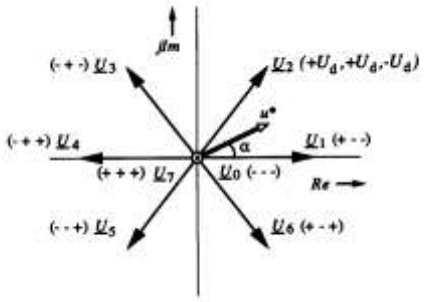
SVM PWM Technique

The Pulse Width modulation technique permits to obtain three phase system voltages, which can be applied to the controlled output. Space Vector Modulation (SVM) principle differs from other PWM processes in the fact that all three drive signals for the inverter will be created simultaneously. The implementation of SVM process in digital systems necessitates less operation time and also less program memory.

The SVM algorithm is based on the principle of the space vector u*, which describes all three output voltages ua, ub and uc :

$$u^* = 2/3 \cdot (ua + a \cdot ub + a2 \cdot uc) \quad \ldots\ldots\ldots(5)$$

Where a = -1/2 + j . v3/2 We can distinguish six sectors limited by eight discrete vectors u0…u7 (fig:- inverter output voltage space vector), which correspond to the 23 = 8 possible switching states of the power switches of the inverter.



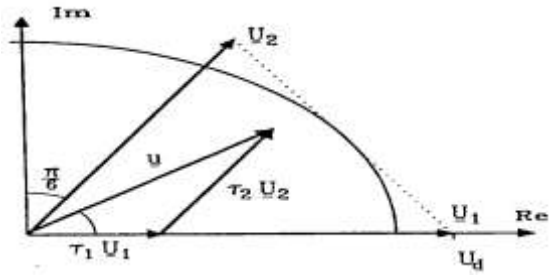
Space vector Modulation

The amplitude of u0 and u7 equals 0. The other vectors u1…u6 have the same amplitude and are 60 degrees shifted.

By varying the relative on-switching time Tc of the different vectors, the space vector u* and also the output voltages ua, ub and uc can be varied and is defined as:

$$ua = Re (u^*)$$
$$ub = Re (u^* \cdot a\text{-}1)$$
$$uc = Re (u^* \cdot a\text{-}2) \quad \ldots\ldots\ldots\ldots(6)$$

During a switching period Tc and considering for example the first sector, the vectors u0, u1 and u2 will be switched on alternatively.



Definition of the Space vector

Depending on the switching times t0, t1 and t2 the space vector u* is defined as:

$$u^* = 1/Tc \cdot (t0 \cdot u0 + t1 \cdot u1 + t2 \cdot u2)$$
$$u^* = t0 \cdot u0 + t1 \cdot u1 + t2 \cdot u2$$
$$u^* = t1 \cdot u1 + t2 \cdot u2$$

Where

$$t0 + t1 + t2 = Tc \text{ and}$$
$$t0 + t1 + t2 = 1$$

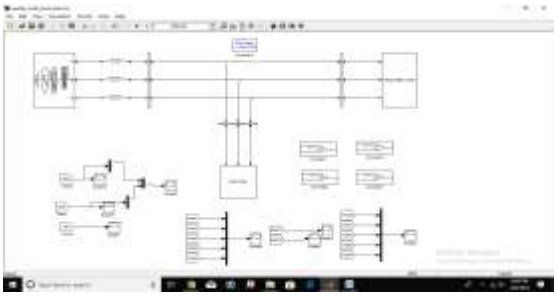
t0, t1 and t2 are the relative values of the on switching times.

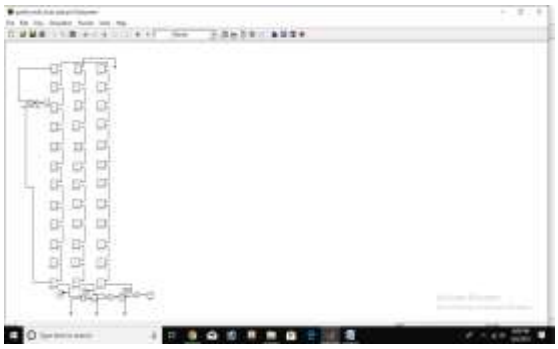
They are defined as: $t1 = m \cdot \cos (a + p/6)$

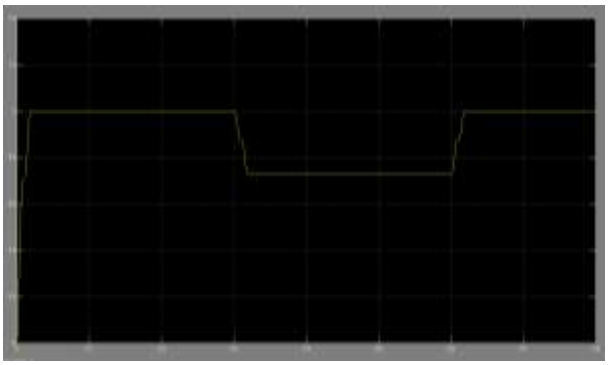
$$t2 = m \cdot \sin a$$
$$t0 = 1 - t1 - t2$$

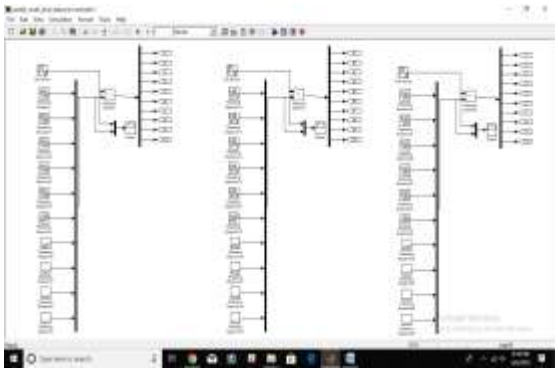
Their values are implemented in a table for a modulation factor m = 1. Then it will be easy to calculate the space vector u* and the output voltages ua, ub and uc. The voltage vector u* can be provided directly by the optimal vector control laws w1, v_{sa} and v_{sb}. In order to generate the phase voltages ua, ub and uc corresponding to the desired voltage vector u* the following SVM strategy is proposed.

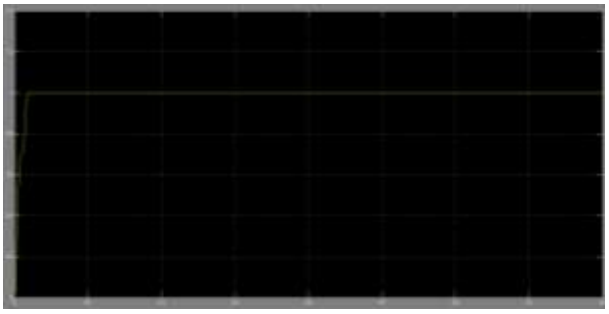
SIMULATION RESULTS

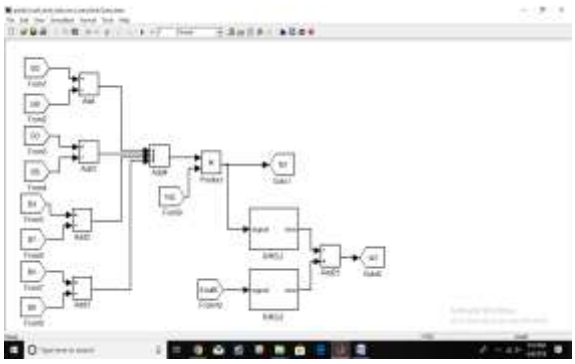


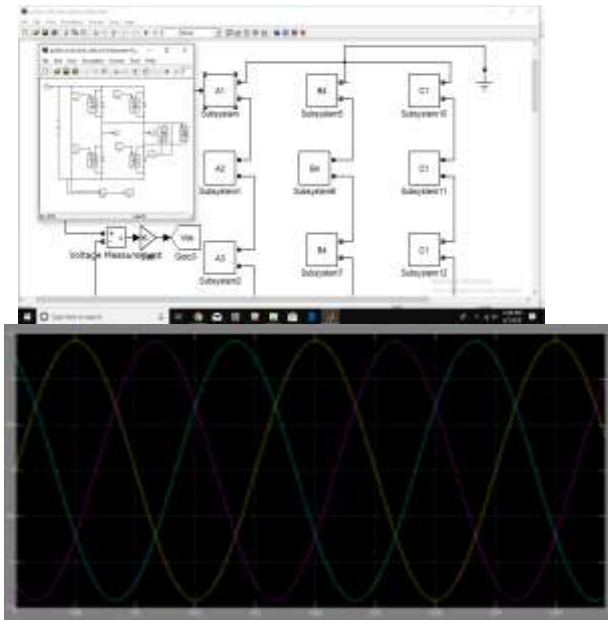












APPLICATIONS OF MATLAB

The accompanying are the uses of MATLAB

1. Calculus. 2.Linear variable based math. 3. Probability and measurements. 4.MATLAB is for unadulterated math or designing purposes, as well as has many applications in funds. 5.MATLAB dialect underpins the vector and framework operations that are fundamental to building and logical issues

Fig. 7.4 demonstrates the reproduction comes about for various working condition. The recreation comes about for change in insolation level and voltage variety at CPI are appeared. The recreations are done in MATLAB simulink and sim control framework tool compartment. The SPV cluster of 25 kW is considered for reenactment examine

CONCLUSION

This paper presents a parallel connected DCM2C-STATCOM system. Based on the

traditional MMC topology, the proposed DCM2C uses clamping diodes to keep the SM capacitor voltages balanced. The main advantage of this topology is that the quantity of capacitor voltage sensors is significantly reduced and the balancing control method is very simple. Furthermore, the capacitor voltage balance speed is fast. Although extra clamping diodes and inductors are required in the novel topology than that of the traditional MMC, the current rating of the diodes and inductors is much lower than the current rating of the main power branch of the converter. So, the cost of DCM2C is not much higher than that of the traditional MMC. With the proposed power control strategy, the DCM2CSTATCOM system can realize Var compensation and negativesequence current compensation. The practical work was performed on a laboratory prototype. Experimental results have verified the effectiveness of the DCM2C topology along with the proposed power control strategy.

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