CASCADED CONTROL SYSTEM OF THE MODULAR MULTILEVEL CONVERTER FOR FEEDING VARIABLE-SPEED DRIVES

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Abstract:
The modular multilevel converter (MMC) is an upcoming topology for high-power drive applications especially in the medium voltage range. This paper presents the design process of a holistic control system for a MMC to feed variable-speed drives. First, the design of the current control for the independent adjustment of several current components is derived from the analysis of the equivalent circuits. Second, the current and voltage components for balancing the energies in the arms of the MMC are identified systematically by the investigation of the transformed arm power components. These fundamentals lead to the design of the cascaded control structure, which allows the balancing task in the whole operating range of a three-phase machine. The control system ensures a dynamic balancing of the energies in the cells of the MMC at minimum necessary internal currents over the complete frequency range. Simultaneously, all other circulating current components are avoided to minimize current stress and additional voltage pulsations. The performance of the control system is finally validated by measurements on a low-voltage MMC prototype, which feeds a field-oriented controlled induction machine.

Keywords: *cascade control, multilevel inverter, current suppression control, variable-speed drives*

INTRODUCTION

The Inverter is an electrical device which converts direct current (DC) to alternate current (AC). The inverter is used for emergency backup power in a home. The inverter is used in some aircraft systems to convert a portion of the aircraft DC power to AC. The AC power is used mainly for electrical devices like lights, radar, radio, motor, and other devices.

DECOUPLED CURRENT CONTROL OF THE MMC

The circuit topology of the presented parallel connected MMCs. The configuration of both MMCs is identical, where each MMC consists of six converter arms, which are constructed by a cascaded connection of SMs with a buffer inductor connected in series. As shown in Fig.1, a half-bridge converter and a dc capacitor constitute the SM, where the terminal between two switches (IGBT1 and IGBT2) and the negative dc-rail terminal will connect to the adjacent SMs to form the aforementioned cascaded connection of single converter arm. And one phase leg consists of two arms, which are named as the positive arm and the negative arm, respectively. The buffer inductors *Ls* limit the circulating currents among six phase-legs in the parallel-MMCs.

The general control diagram of parallel-MMCs for grid-tied applications is illustrated in Fig.3, where the general control function is realized by the voltage-balancing control blocks and circulating current suppression control (CCSC) blocks forMMC 1 and MMC 2 and the external ZSCC control block. The decoupled

current control block is assumed to generate the fundamental control reference in the grid-tied applications, which may vary depending on the application cases. A general three phase PLL is assumed to obtain the phase angle, which is not drawn in Fig.3. In what follows, we will illustrate the capacitors voltage balancing control method in detail, whose control principle is suitable for the parallel-MMCs operated under both the normal operation condition and the switch fault-tolerant operation conditions.

For tuning multiple harmonics, although the resonant controllers placed in the stationary reference frame can be used, they would result in more terms for summation. Therefore, as an alternative, the resonant controllers in the synchronous reference frame would be more effective, since each represents two equivalent resonant terms in the stationary reference frame for compensating two harmonics simultaneously as stated in. According to the circulating currents analysis in, the second-order current harmonic is a negative-sequence current, the fourth-order current harmonic is a positive-sequence current, and the sixth-order harmonic is a zero sequence current. Thus, the three-phase second- and fourth-order current harmonics can be tuned simultaneously by only using two third-order

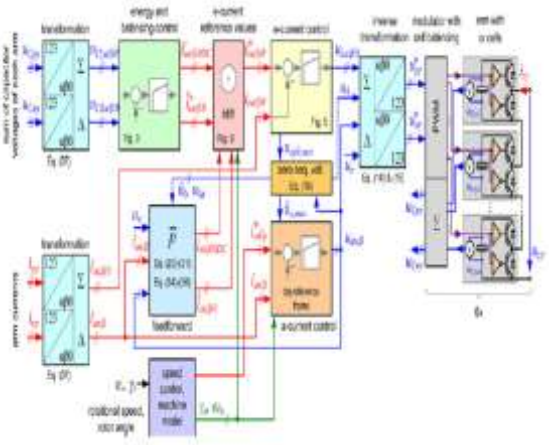

Fig 1: Signal flow path of complete MMC control system with subordinate current controllers, arm energy balancing, motor control unit, and modulator.

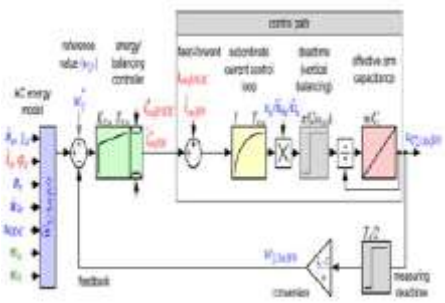

Fig 2: Illustration of the positive-sequence decoupled current control block.

resonant controllers to, respectively, tune the transformed *dq* components under the synchronous reference frame as shown in Fig.5. In order to suppress the sixth-order zero sequence current harmonic, an additional resonant controller is assumed to suppress the summed three-phase current in Fig. 5. The assumed resonant controllers can be, respectively, written As where $K3$,$K6$, and $\omega 0$ represent the integral gains and the fundamental frequency, respectively.

$$\begin{cases} G(s) = \dfrac{K_3 s}{s^2 + (3\omega_0)^2} \\ G(s) = \dfrac{K_6 s}{s^2 + (6\omega_0)^2} \end{cases}$$

The summed control signal per SM in the positive-arm and the negative-arm can be written as where *vj px* and *vj nx* (*x* = *a*, *b*, or *c*, *j* = 1 or 2) are the primary control commands derived from the current control block in Fig. 3, whose detailed control diagram is drawn in Fig.6, where the three-phase control signals *vj px* and *vj nx* will be assigned to control six arms per MMC to track the current reference.

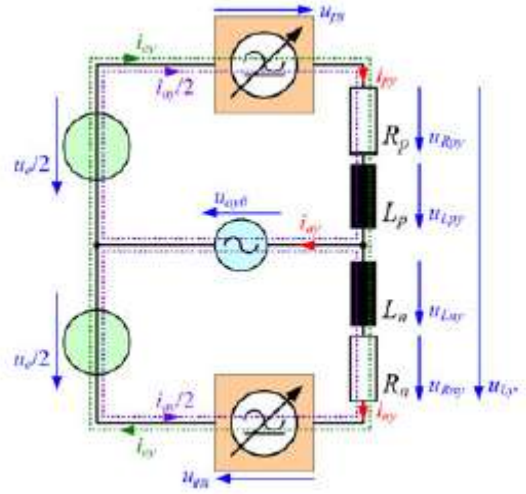

Fig 3: Equivalent circuit of one phase of the MMC.

CONTROL SYSTEM OF THE MMC FOR VARIABLE-SPEED DRIVES

The SM can be treated as a controlled voltage source when building the average model of parallel-MMCs. According to the analysis in [16], *px*1 and *nx*1 (*x* = *a*, *b*, or *c*) are the virtual equipotential points in Fig. 2. Therefore, both buffer inductors per phase can be treated as the parallel connected inductors in Fig. 7, where it is easy to obtain *L*1 = *LS*1 /2, *L*2 = *LS*2 /2. The sum of capacitor voltages in positive arm and negative arm per phase are equivalent to the controlled voltage *Uj px* and *Uj nx* (*x* = *a*, *b*, or *c* and *j* = 1 or 2)

$$\begin{cases} u_{px}^{j} = \sum_{i=1}^{n} S_{pxi}^{j} U_c \\ u_{nx}^{j} = \sum_{i=1}^{n} S_{nxi}^{j} U_c \end{cases}$$

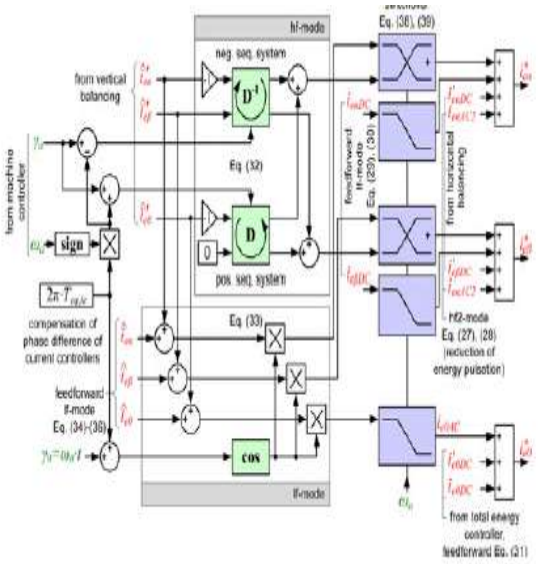

Fig 4: Estimation of the e-current reference values.

FAULT-TOLERANT OPERATION OF PARALLEL-MMCS

In view of the high amount of power semiconductors in the parallel-MMCs, any failure can cause large downtime and tremendous losses for the consumers. Therefore, it is important to develop the fault-tolerant operation schemes to enhance the reliability. This paper proposes the novel PWM compensation schemes for the fault-tolerant operation of parallel-MMCs without using an additional backup hardware. Only single-switch fault in one SM is considered in this paper, whose failure conditions can be broadly classified as the open-circuit fault and short-circuit

fault. Carefully analyzing the switching states per SM in Fig. 1, it is noted that the open-circuit fault of IGBT 1 and the short-circuit fault of IGBT 2 are identical for the fault-tolerant operation and similarly the short-circuit fault of IGBT 1 and the open-circuit fault of IGBT 2 are identical either in terms of their complementary switching sequence. Therefore, the fault-tolerant operation of parallel-MMCs only needs to consider two cases: open-circuit fault and short-circuit fault of IGBT 1.

PWM Compensation Schemes for the Open-Circuit Fault-Tolerant Operation of IGBT 1

Once the IGBT 1 suffers the open-circuit fault, the whole SM is recommended to only output state *{0}* by keeping IGBT 2 ON in order to maintain the continuous arm current being
equivalent to the bypass function of SMs. In this case, the corresponding phase arm will lose one voltage level. In order to reduce the circulating current induced by the absence of one
SM, it is suggested that the corresponding opposite phase arm downgrade its switching level from $N + 1$ to N either. And the healthy SM capacitor voltages in the faulty phase-leg should be slightly increased to $NUc/(N-1)$ so that the summed phase voltage is still equal toNUc the same as that of other two healthy phase-legs. Doing so, the revised switching states in the faulty phase-leg would not induce any additional circulating current in theory. The switching level reduction in the faulty phase-leg can increase the output harmonics induced by the unbalanced output line voltages. Reducing the switching level of other five healthy phase-legs with or without increasing their SM capacitor voltages can keep the balanced output line voltage as an alternative.

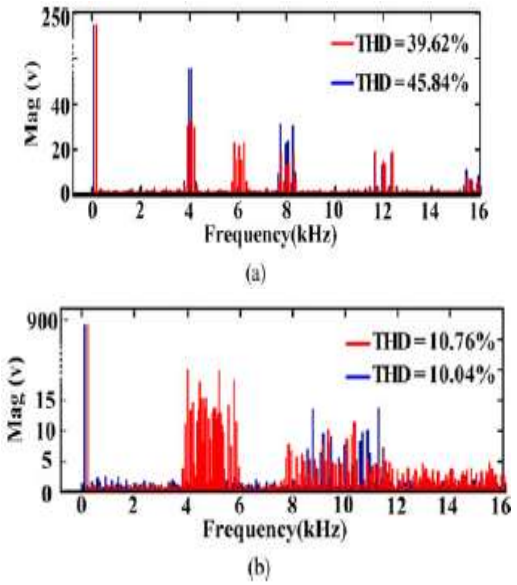

Fig 5: Harmonics spectrum and THD of line-voltages between phase A and B

the line voltage THD and harmonic spectrum of the aforementioned two PWM compensation methods. It is revealed that the output quality of the former method for only reducing the switching level of faulty phase-leg could have a better output quality compared to the latter method when the number of SM is less. Comparatively, when the number of SM increases, the latter method could demonstrate the better output quality as

Besides, the aforementioned two fault-tolerant operation schemes could demonstrate the different merits and demerits for the different applications. For the cases with the invariant dc-link voltage, e.g., the rear-end inversion part of HVDC, the fault-tolerant operation scheme with the switching level downgrade of only faulty leg is superior since it would minimize the dc-link inrush current during the transit process. For the cases, where the dc-link voltage is allowed to reduce

accordingly, e.g., the reactive power compensation system with the redundant SMs, it is recommended to downgrade the switching level of all six phase-legs in parallel-MMCs without inducing the high inrush current and meanwhile keeping the superior output performance.

Revised Control Scheme for the Short-Circuit Fault-Tolerant Operation of IGBT 1

Unlike the H-bridge SM, the half-bridge SM does not have the redundant switching states to bypass the faulty switch. When the IGBT 1 suffers the short-circuit failure, the corresponding SM must keep its output state *{1}* unchanged, which would unavoidably insert the dc capacitor

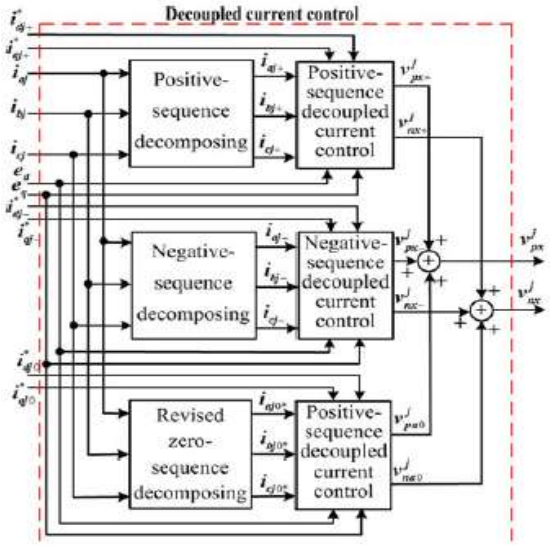

Fig 6: Illustration of positive-, negative-, and zero-sequence currents decoupled control block.

into the load current flowing loop resulting in the damageable overvoltage breakdown. Therefore, when such short-circuit failure happens, the corresponding whole phase arm should be shut down to protect the equipment. Traditionally, the single three-phase MMC cannot continue its normal operation since one phase-leg is out of operation. But fortunately, the parallel-MMCs provide the redundant phase-leg to ride-through the short-circuit failure condition with the careful consideration of tradeoff between the current rating and the output power.

As a consequence, the parallel-MMCs will continue its operation by only using five phase-legs. In order to maintain the symmetrical three-phase output currents, the corresponding phase leg in the healthy MMC can generate double output current with
the output current of other four legs unchanged to produce the same output power as that before the switch failure. For example, assuming that the total three-phase output currents are
ia, ib , and *ic* , respectively, and an SM of phase A in MMC 1 suffers the IGBT 1 short-circuit failure condition, the phase A in MMC 2 would produce the output current of *ia* , while the
other four healthy phases would generate 12 *ib* , 12 *ic* , 12 *ib* , and 12 *ic* , respectively, as usual to make sure that the total three-phase currents are symmetrical as expected. In this case, the desired output currents per MMC are unbalanced. Therefore, the traditional decoupled positive-sequence current control method for the grid-tied applications illustrated in Fig. 6 cannot be solely employed to control the output currents since the unbalanced
three-phase currents per MMC can be decomposed into the positive-sequence, negative-sequence, and zero-sequence components. A combined closed-loop current controller is shown in Fig. 11

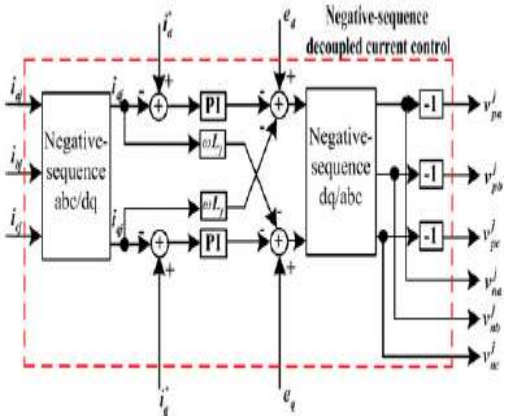

Fig 7: Illustration of negative-sequence decoupled current control block.

Diagnostic Methods for the IGBT Faults and the Reconfigured Control Logic

Diagnostic methods for the IGBT faults have been presented in many published literature works. Park's vector approach as an effective fault diagnostic tool for voltage source inverter was first proposed in. The localization of the faulty switch can also be identified by the analysis of the current space-vector trajectory diameter. A novel fast-diagnostic method for open-circuit faults without sensors is proposed to improve the reliability of the power electronic system in. Estima and Cardoso present a new diagnostic method that allows the real-time detection and localization of single-power switch open-circuit faults in VSI-fed PWM motor drives. Besides, the fault detection methods in multilevel converters include the frequency analysis method neural networks method and load voltages and currents time behavior methods . The fault detection interval may vary from few switching periods to few milliseconds as indicated in and Regardless of the specific fault detection principle, the inherent current limit characteristics of the MMC can indeed help reduce the transient damage. The next step is to reconfigure the switching sequences and control function in order to minimize the performance degradation as illustrated in Section V-A and V-B. Since the gate driver can directly detect the IGBT short-circuit fault and clamp the switching commands of opposite IGBT in a half-bridge module, the reconfigured control function for IGBT 1 short-circuit fault could be immediately implemented upon the controller receiving the feedback fault signal. For another case, where IGBT 1 suffers the open-circuit fault, the complicated switching logic reconfiguration should be implemented as illustrated below.

SIMULATION RESULTS

To verify the theoretical findings presented in this paper, the simulation model of parallel-MMCs with three SMs per phase arm was built in MATLAB/Simulink. The carrier phase-shifted modulation method was assumed. To simulate the different power consumption among all SMs, an equivalent resistor was connected to the capacitor per SM in parallel with the value of 500, 700, and 800 Ω in the positive arm, and 400, 500, and 700 Ω in the negative arm, respectively. The circuit parameters

CIRCUIT PARAMETERS:

DC bus voltage	U_{dc}	600V
Sub-module capacitor voltage	U_C	200V
Sub-module capacitor	C	3300uf
Fundamental frequency	f	50Hz
Carrier frequency	f_C	5kHz
Output filter inductances	L_{01}	2mH
	L_{02}	5mH
Buffer inductances	L_{s1}	2mH
	L_{s2}	2mH
Output phase voltage (RMS)	U_s	110V

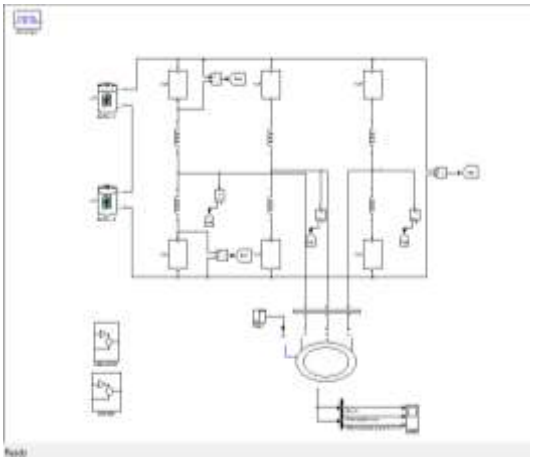

Fig 8: simulation model of proposed mmc with variable speed drive

are listed in Table I, where the output filter inductances are different. The *d*- and *q*-axis current references *id* and *i q* in Fig. 6 are set to be 30 and 30 A, respectively, under both the normal and switch fault operation conditions. To verify the voltage-balancing control method under the normal operation conditions, the simulated capacitor voltages of the positive arm and negative arm are shown in Fig. 13. It is obvious that the voltage balancing control method works well and all capacitor voltages are balanced around 200 V as expected. A little bit unbalanced voltage (around 3 V) will appear in the capacitors of MMC 1 since the external ZSCC control signal is added in the control loop of MMC 1. But, the small unbalanced voltage is still within the acceptable range.

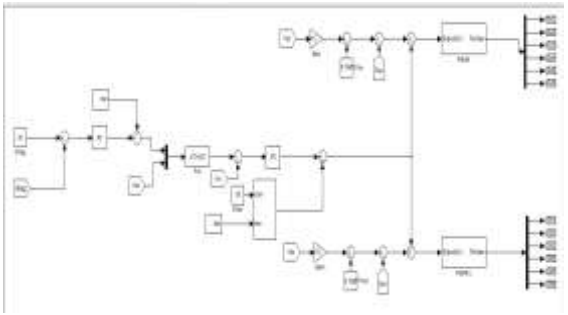

Fig 9:effective control loop for balancing the arm energies of the MMC.

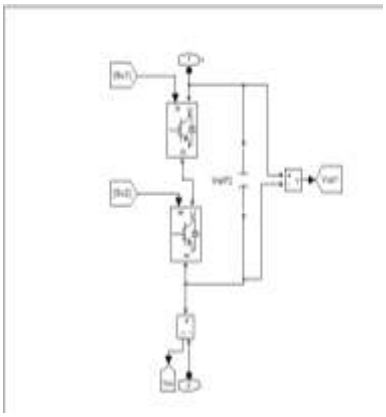

Fig 10: single cell model of mmc

the simulated internal circulating currents and their spectrum in MMC 1 without and with the proposed CCSC method added under the normal operation conditions. It is noted that the internal circulating currents without using the proposed CCSC method contain the dominant low-frequency second-, fourth-, and sixth-order current harmonics as shown in Fig. 14(a) and (b). By using the proposed CCSC method, the low-frequency harmonics are significantly suppressed as shown in Fig. 14(c) and (d). It can also be seen that the positive-arm and negative-arm currents have become near sinusoidal by employing the proposed CCSC method as shown in Fig. 15.

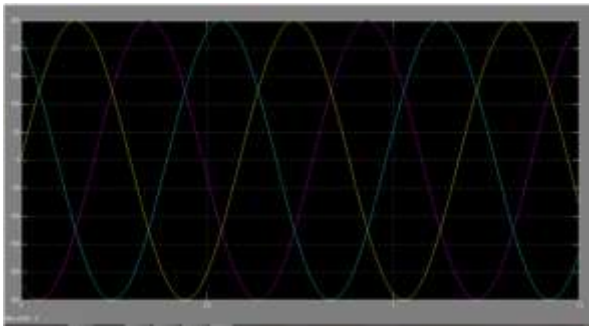

Fig 11:inductive currents of cascaded mmcs

In order to verify the performance of the ZSCC control method in the parallel-MMCs, Fig. 16(a) shows the simulated ZSCC without using the ZSCC control method, where the ZSCCs *i*01 and

*i*02 are apparently large. In comparison, Fig. 16(b) shows the simulated results with ZSCC control added, where the ZSCCs are almost eliminated. In addition, Fig. 17 shows the phase A currents *ia*1 and *ia*2 of MMC1 and MMC2 and their difference under the operation conditions without and with the ZSCC control method added, respectively. Obviously, using the ZSCC control method can significantly reduce the phase current difference between MMC1 and MMC2.

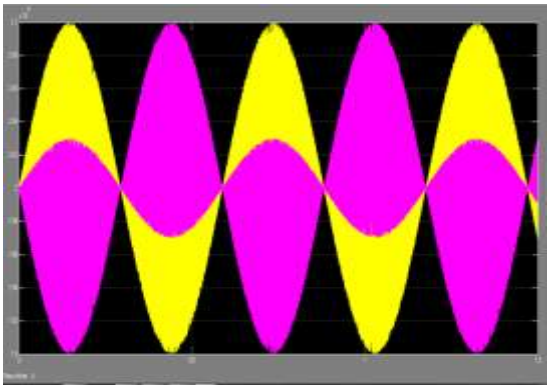

Fig 12: phase voltages of cascaded mmc

Fig. 18 shows the simulated results of parallel-MMCs under the fault-tolerant operation condition when IGBT 1 in phase A of MMC 1 suffers the open-circuit failure at 0.59 s and the switching sequence is reconfigured at 0.6 s by fully considering the time delay induced by the fault detection algorithm and communications. It is noted that the healthy SM capacitor voltages in the faulty phase-leg are now charged to 300 V and others still remain 200 V as shown in Fig. 18(a). Fig. 18(b) and (c) shows that the phase A of MMC 1 produce a reduced level phase voltage while the phase voltages of phase B and C remain unchanged. Fig. 18(d) shows the three-phase output currents of MMC 1, which are quickly attenuated to be balanced after the switch failure. Fig. 18(e) and (f) shows the internal circulating currents ofMMC1 and the external circulating currents, respectively. It is noted that all circulating currents can be successfully suppressed again after the switch failure. Due to the inherent current limit characteristics, the fault detection and communication delays will not induce severe transient performance downgrade.

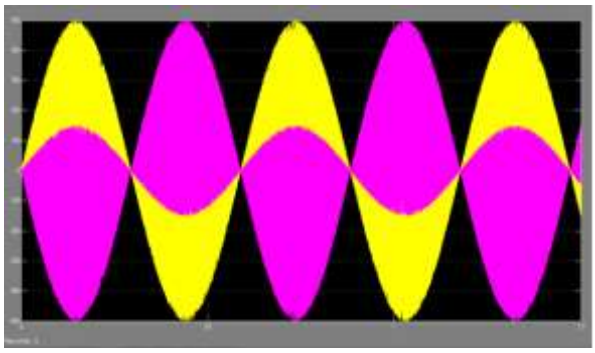

Fig 13: phase currents of cascaded mmcs

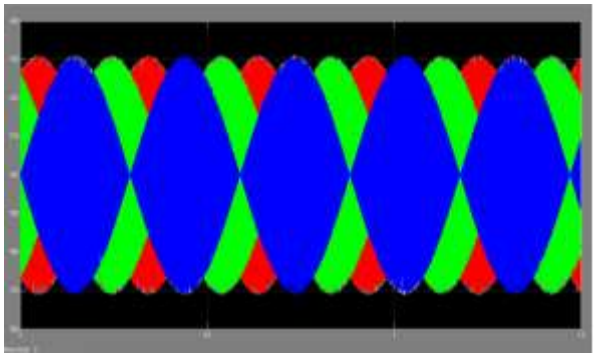

Fig 14: capacitor voltages of modular multilevel converters

Fig. 19 shows the simulated results of parallel-MMCs under the fault-tolerant operation condition when IGBT 1 in phase A ofMMC1 suffers the short-circuit failure at 0.59 s. Similarly, the added time delay is 10 ms for reconfiguring the control function. As presented in Section V-B, the faulty phase-leg should be shut down to avoid the overvoltage damage. Therefore, the phase A current in MMC 1 is now reduced to zero and as a consequence the phase A current in MMC 2 continuously increases to reach its double value leaving other four phase currents unchanged as

shown in Fig. 19(a) and (b). Therefore, the total output current can keep unchanged as expected as shown in Fig. 19(c). The current difference between two MMCs is shown in Fig. 19(d), where the zero current difference in phase B and C verifies that the external ZSCC control block can be removed when the parallel-MMCs switches to the five-leg operation conditions. The SM capacitor voltages of MMC 1 and MMC 2 are shown in Fig. 19(e) and (f), respectively. Note that only the capacitor voltages in phase A of MMC 2 are increased because a larger phase current flows through the corresponding SMs. The internal circulating currents ofMMC1 andMMC2 are shown in Fig. 19(g) and (h), respectively. It is found that only the internal circulating currents of phase A in MMC 2 have obviously increased since its corresponding SM capacitor voltages are varying in a wider range as shown in Fig. 19(f).

CONCLUSION

A cascaded control system for the MMC to feed variable speed drives is derived on the base of the analysis of the equivalent circuit as well as of the active power components in the arms. The realization by the transformation of all relevant values allows a dynamic control of the arm energies over the complete operation range of the drive at minimum internal currents. The systematical design process of the several controllers and feed-forward components for the balancing tasks are presented. Finally, the measurement at a MMC prototype combined with a field-oriented control of an induction machine validates the approach and illustrates the performance of the control system. The proposed control and balancing system of the MMC allows the supply of three-phase machines independent of their type and motor control system.

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