DESIGN OF A PARALLEL SELF TIMED ADDER BY USING RECURSIVE APPROACH

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ABSTRACT:

Adders being core building blocks in different VLSI circuits like microprocessors, ALU's etc. performance of adder circuit highly affects the overall capability of the system. In this paper we present the design and performance of Parallel Self-Timed Adder. It is based on a recursive formulation for performing multi-bit binary addition. The operation is parallel for those bits that do not need any carry chain propagation. A practical implementation is provided along with a completion detection unit. The implementation is regular and does not have any practical limitations of high fanouts. The proposed work mainly aimed at minimizing the number of transistors and estimation of various parameters viz., area, power, delay for Parallel Self-Timed Adder (PASTA). We have also designed 4 bit PASTA as an example of proposed approach.

Keywords: *Binary adders, Parallel, Adders, Asynchronous circuits, CMOS design.*

I. INTRODUCTION

Addition is the most common and often used arithmetic operation in microprocessor, digital signal processor, especially digital computers. Also, it serves as a building block for synthesis all other arithmetic operations. Thus performance of any circuit is mainly determined by speed of adder circuit. Circuits may be classified as synchronous or asynchronous. Synchronous circuits are based on clock pulse whereas an asynchronous circuit, or self-timed circuit, is not governed by a clock circuit or global clock instead; they often use signals that indicate completion of operations. Such a system tends to have better noise and electromagnetic compatibility properties than synchronous systems due to the absence of a global clock reference.

Asynchronous operation by itself does not imply low power, but often suggests low power opportunities based on the observation that asynchronous circuits consume power only when it is active. The synchronous adders perform slowly due to its incremental nature of operation and therefore it is not recommended for fast and parallel adders. The basic building block of combinational digital adders is a single bit adder. The simplest single bit adder is a half adder (HA). The full adders (FA) are single bit adders with the carry input and output. The full adders are basically made of two half adders in terms of area, interconnection and time complexity. This paper proposes the design of parallel self timed adder

(PASTA). The design of PASTA is regular and uses half adders along with multiplexers with minimum interconnection requirement. The interconnection and area requirement is linear which makes it feasible to fabricate in a VLSI chip. The design operates in a parallel manner for those bits that do not require any carry propagation. It is self timed, which means that as soon as the addition is done, it will signal the completion of addition thereby overcoming the clocking limitations.

II. SELF-TIMED ADDERS

Self-planned alludes to rationale circuits that rely on upon timing suppositions for the right operation. Self-coordinated adders can possibly run speedier arrived at the midpoint of for element information, as early fulfillment detecting can maintain a strategic distance from the requirement for the most pessimistic scenario packaged defer component of synchronous circuits.

A. PIPELINED ADDERS USING SINGLE-RAIL

Information Encoding: The offbeat Req/Ack handshake can be utilized to empower the snake obstruct and also to set up the stream of convey signs. In the vast majority of the cases, a double rail convey tradition is utilized for inside bitwise stream of convey yields. These double rail signs can speak to more than two rationale values (invalid, 0, 1), and along these lines can be utilized to create bit-level affirmation when a bit operation is finished. Last finish is detected when all piece Ack signs are gotten (high). The convey fruition detecting viper is a case of a pipelined snake, which utilizes full viper (FA) useful pieces adjusted for double rail convey.

Then again, a theoretical fruition viper is proposed. It utilizes purported prematurely end rationale and early fruition to choose the correct culmination reaction from various settled postpone lines. In any case, the prematurely end rationale usage is costly because of high fan-in necessities.

B. DELAY INSENSITIVE ADDERS USING DUAL

Rail Encoding: Defer uncaring adders are offbeat adders that state packaging limitations or Delay Insensitive (DI) operations. In this manner, they can effectively work in nearness of limited yet obscure entryway and wire postpones. There are numerous variations of DI adders, DI adders utilize double rail encoding and are expected to expand intricacy. In spite of the fact that double rail encoding duplicates the wire many-sided quality, they can in any case be utilized to deliver circuits almost as productive as that of the single-rail variations utilizing dynamic rationale or MOS just outlines.

Along these lines, they can possibly work speedier when there is long convey chain. A further enhancement is given from the perception that double rail encoding rationale can profit by settling of either the 0 or 1 way. Double rail rationale requires not sit tight for both ways to be assessed. In this manner, it is conceivable to further accelerate the convey look-ahead hardware to send convey create/convey execute signs to any level in the tree.

III. PROPOSED SYSTEM

A. Architecture of PASTA:

The general block diagram of the Parallel Self-Timed Adder (PASTA) is presented in Fig.1. Multi bit adders are often constructed from single bit adders using combinational and sequential circuits for asynchronous or synchronous design.

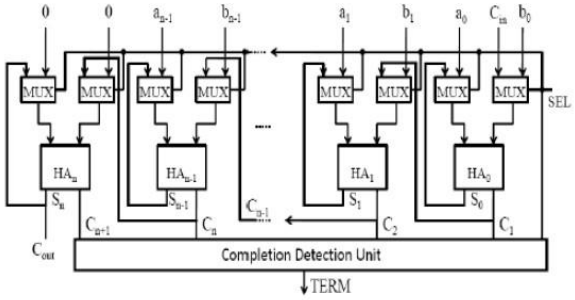

Fig1: General block diagram of Parallel Self-Timed Adder

The selection input for two-input multiplexers corresponds to the Req handshake signal and will be a single 0 to 1 transition denoted by SEL. It will initially select the actual operands during SEL = 0 and will switch to feedback/carry paths for subsequent iterations using SEL = 1. The adder first accepts two operands to perform half-additions for each bit. Subsequently, it iterates using earlier generated carry and sums to perform half-additions repeatedly until all carry bits are consumed and settled at zero level.

B. State Diagrams: In Fig.2, two state diagrams are drawn for the initial phase and the iterative phase of the proposed architecture. Each state is represented by (*Ci*+1 *Si*) pair where *Ci*+1, *Si* represent carry out and sum values, respectively, from the *i*th bit adder block. During the initial phase, the circuit merely works as a combinational HA operating in fundamental mode. It is apparent that due to the use of HAs instead of FAs, state *(*11*)* cannot appear. During the iterative phase (SEL = 1), the feedback path through multiplexer block is activated. The carry transitions (*Ci*) are allowed as many times as needed to complete the recursion.

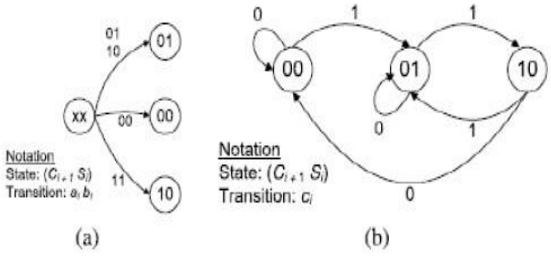

Fig-2: State diagrams for PASTA. (a) Initial phase. (b) Iterative phase.

IV.RESULTS

Fig.3 RTL Schematic

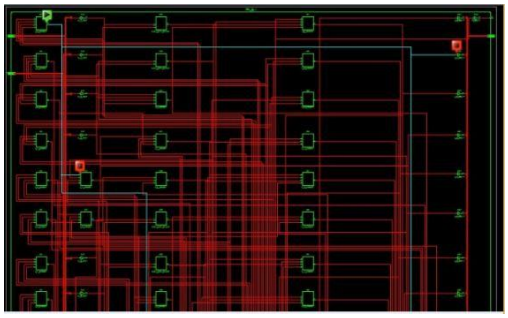

Fig 4. Technology Schematic

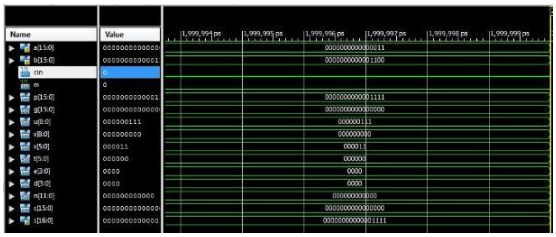

Fig5. Output Waveform

V. CONCLUSION

In this paper we implemented the Modified PASTA. Subsequently, the architectural design and CMOS implementations for Parallel Self-Timed Adder are presented. The new design using transmission gate and CMOS transistor is proposed and implementation is done using CMOS technology. With the proposed design, the reduction in number of transistor count is achieved as compared with previous CMOS implementation of PASTA. This achieves a very simple n-bit adder that is area, power consumption wise much more efficient than the previous self timed adder Moreover, the circuit works in a parallel manner for independent carry chains, and thus achieves logarithmic average time performance over random input values. The completion detection unit for the proposed adder is also practical and efficient. Simulation results are used to verify the advantages of the modified self timed adder.

VI. REFERENCES

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