A TWO-LEVEL DEAD-TIME INSERTED SVPWM ALGORITHM FOR FIELD-ORIENTED CONTROLLED INDUCTION MOTOR DRIVE

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ABSTRACT

New Space vector pulse width modulation (SVPWM) technique to control the voltage source inverter is presented in this paper. Many types of Pulse width modulation (PWM) techniques have been determined in recent times to control the Voltage source inverter (VSI) fed induction motor drive. These PWM algorithms requires additional circuits such as dead band circuit or special protection circuits for real time implementation to prevent the mis-operation of inverter. But this complete experimental set up will increase the complexity of circuit. Here we introduce the new SVPWM i.e.., we insert the integrated dead time in SVPWM algorithm in the range of micro seconds with help of high speed processors. Hence a new integrated dead time space vector pulse width modulation (IDTSVPWM) algorithm has been simulated in the MATLAB environment and also presents the hardware work for experimental validation i.e.., a prototype hardware kit of STM32F4 cortex M4 processor for 1hp induction motor.

Keywords— *Space vector pulse width modulation (SVPWM); Integrated dead time (IDT); voltage source inverter (VSI); pulse width modulation (PWM);*

I. INTRODUCTION

Modern age technology development in the area of inverter fed induction motor drives has led to the scenario where the swift pace of working of the drives is required. Selecting a suitable configuration for fast dynamic performance and accurate control strategy of inverter using PWM techniques [1] is reported in the recent past research work. In [2] the effect of noise due to harmonics is dealt in detail for inverter fed induction motor drives. Further in [3] the effect of dead-time on oscillations and performance of the induction motor drive is discussed. The motor acoustic noise based on different advanced bus clamped PWM control algorithms is presented in [4]. A mechanism to reduce the current ripple using PWM is described in [5]. In [6] an improved flux and torque performance of DTC based induction motor drive is presented. MRAS based DTC of induction motor drive has been presented in [7]. Different Bus Clamped PWM algorithms to generate the duty ratios of the inverter have been represented in [8]. A comparison of carrier based and conventional SVPWM has been dealt in detail in [9]. A three-level NPC inverter with Neuro-fuzzy based SVPWM has been implemented in [10]. In this paper a generalized dead time insertion algorithm has been designed which is implemented for SVPWM based two-level inverter fed induction motor drive.

II. INTEGRATED DEAD TIME SVPWM

Actually the two parameters such as sampling time(T_s) and carrier frequency(f_c) are important for implementing the SVPWM algorithm. Therefore it is necessary to determine the sampling time(T_s) and carrier frequency(f_c) before the dead time (t_d) inserted in the SVPWM. The change in above parameters will affect the steady state performance parameters such as THD, torque ripple, flux and stator current of induction motor drive. Therefore the duty ratios are modified in such a way that they are independent of T_s and f_c. In this way a new modified SVPWM algorithm has been developed, with the help this new SVPWM technique an integrated dead time insertion block is used which inserts specified t_d for given T_s and f_c by taking the three phase duty ratios as

inputs. This block hence is inserted in between duty ratios generator and inverter as shown in Fig. 1. So that the new gate pulse which we required are fed to the inverter.

Finally, complete IDTSVPWM block takes the three- phase balanced reference sinusoidal reference signals as inputs and generates the six gate pulses for two-level inverter with integrated dead time.

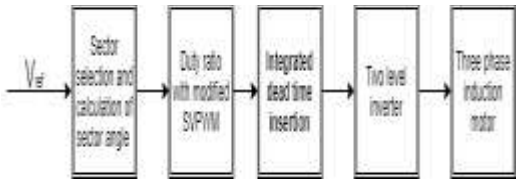

Fig.1. Block diagram of Integrated Dead-Time SVPWM fed IM Drive.

A. Description of conventional SVPWM

SVM is the preferred real time pwm technique and is mostly used for digital control of VSI's.

SVPWM is the best and accurate PWM technique among all the available PWM techniques. SVPWM generates less harmonics in output voltage and current which is applied to three phase AC motor. Another important advantage of SVPWM is more DC bus utilization it means efficient use of DC supply voltage in compared to sinusoidal modulation technique.the dead time is inserted in the SVPWM algorithm to avoid the malfunction of inverter.

The circuit of three phase VSI is shown in fig..,

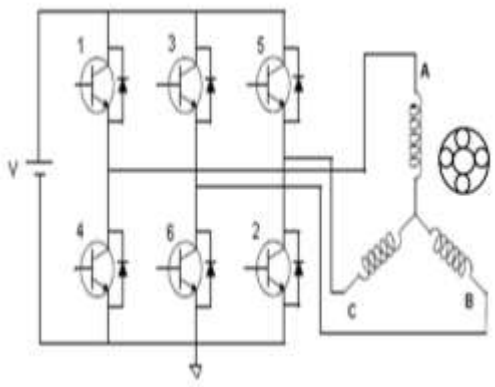

Fig. 2. Circuit diagram of Two-Level Inverter fed Induction Motor

Two level inverter produces the output voltage or current with the levels of 0 or +/- V. The inverter is composed of 6 groups of active switches 1-6. Based on dc operating voltage two or more IGBT or GCT switches connected in series.

SVPWM is inherently a voltage control scheme. With the known reference voltage's space vector, this SVPWM algorithm calculates the optimum switching order for the inverter to ensure that the desired space vector voltage is obtained. These calculations are performed in the α–ß or "space vector" plane.

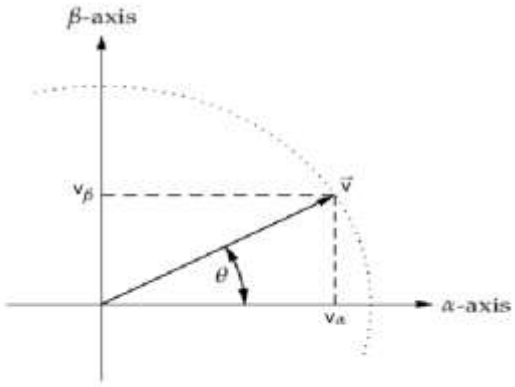

Fig.3. The space vector V in the α−β plane.

With the α−β plane in essence being a 2D plane, this allows us to write the space vectors in a complex form as,

$$\vec{V} = v_\alpha + jv_\beta$$

For the inverter to produce a specific reference voltage (Vref), the inverter have to "make up" this reference vector using only the six available switching vectors and the two zero vectors. If the reference vector is situated in, say sector I, switching vectors$\vec{V_1}, \vec{V_2}$ as well as the two zero switching vectors $\vec{V_0}$, and $\vec{V_7}$,will produce the minimum associated current errors.

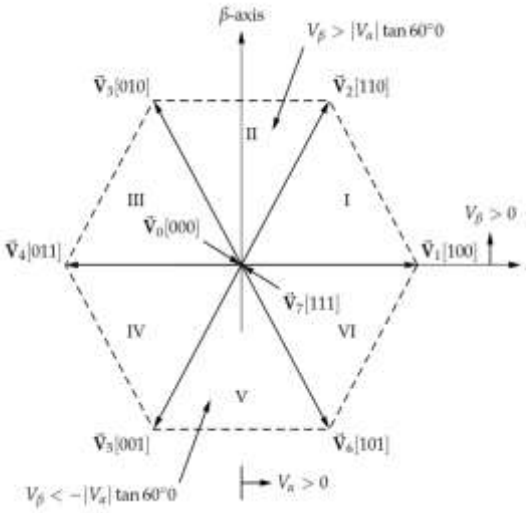

Fig. 3. Space-Vector diagram of Two-Level Inverter

The reference voltage V_{ref} generated by the SVPWM can be expressed in terms of three balanced voltagesV_{AO},V_{BO} and V_{C0} as

$$V_{ref} = V_{AO} \cdot e^{j0} + V_{BO} \cdot e^{j\frac{2\pi}{3}} + V_{CO} \cdot e^{j\frac{4\pi}{3}} \quad \textbf{(1)}$$

The SVPWM now approximates the trajectory of V_{ref} by switching between six active vectors V_1 to V_6 and two null vectors V_0 and V_7, by dividing the circular trajectory of V_{ref} into a no. of samples in the interval of one cycle.

The duration of each vector during one sampling time is obtained by the dwell times. The dwell time duty cycles A, B and C can be obtained as given in equations (2) to (5). These dwell times are calculated based on the volt-sec balancing principle [11]. These dwell times are applied to each of the corresponding switching state in each sampling time interval produces the pulses for each of three legs of the inverter.

$$A = \frac{m.T_s.\left(\sin\frac{\pi}{3} - \alpha\right)}{\sin\frac{\pi}{3}} \quad (2)$$

$$B = \frac{m.T_s.(\sin\alpha)}{\sin\frac{\pi}{3}} \quad (3)$$

$$T_s = A + B + C$$

$$C = T_s - (A + B) \quad (4)$$

$$\text{Amplitude ratio } m = \frac{|V_{ref}|}{\sqrt{\frac{2}{3}}V_{dc}} \quad (5)$$

B. Modified SVPWM for generation of duty ratios

The pulses that are generated for each of the three legs of the two-level inverter are obtained from a duty ratio generator for each of the three phases. The equations (2) to (5) are modified as it may be necessary to treat the equations independent of f_c, T_s and t_d. This new duty ratio's can be obtained by dividing the previous duty ratios a, b, and c with T_s as follows:

$$a = \frac{m.\sin\left(\frac{\pi}{3} - \alpha\right)}{\sin\left(\frac{\pi}{3}\right)} \quad (6)$$

$$b = \frac{m.\sin(\alpha)}{\sin\left(\frac{\pi}{3}\right)} \quad (7)$$

$$c = 1-(a+b) \quad (8)$$

It is observed that the above equations (6) to (8) are independent of sampling period (Ts) and carrier frequency (f_c). They depend on sector angle α and amplitude ratio of inverter. An integrated dead-time insertion block is now used which takes the three phase duty ratios as inputs and produces high pulses AH, BH and CH along with low pulses AL, BL and CL with the required dead time td inserted in between high and low pulses. From the duty ratio D_A, D_B and D_C generated, the high duty ratios and low duty ratios are obtained. This dead time insertion is mandatory for hardware implementation. The dead-time insertion block prevents the dead short-circuit of the two switches of the same leg when the switching action suddenly changes from top switch to bottom switch of a leg and vice-versa. The final obtained duty ratios are now compared with a high frequency carrier waveform with a

switching frequency f_c to obtain gate pulses for inverter.

TABLE I

Sector	Duty ratios
1	$\begin{bmatrix}D_A\\D_B\\D_C\end{bmatrix}=\begin{bmatrix}d_a+d_b+d_c/2\\d_b+d_c/2\\d_c/2\end{bmatrix}$
2	$\begin{bmatrix}D_A\\D_B\\D_C\end{bmatrix}=\begin{bmatrix}d_c/2+d_a\\d_a+d_b+d_c/2\\d_c/2\end{bmatrix}$
3	$\begin{bmatrix}D_A\\D_B\\D_C\end{bmatrix}=\begin{bmatrix}d_c/2\\d_a+d_b+d_c/2\\d_b+d_c/2\end{bmatrix}$
4	$\begin{bmatrix}D_A\\D_B\\D_C\end{bmatrix}=\begin{bmatrix}d_c/2\\d_c/2+d_a\\d_c/2+d_a+d_b\end{bmatrix}$
5	$\begin{bmatrix}D_A\\D_B\\D_C\end{bmatrix}=\begin{bmatrix}d_b+d_c/2\\d_c/2\\d_a+d_b+d_c/2\end{bmatrix}$
6	$\begin{bmatrix}D_A\\D_B\\D_C\end{bmatrix}=\begin{bmatrix}d_c/2+d_a+d_b\\d_c/2\\d_c/2+d_a\end{bmatrix}$

III. INTEGRATED DEAD TIME SPACE VECTOR PWM

The duty ratios obtained from (6), (7) and (8) are to be modified to insert the required dead time. The insertion of dead-time in the top group switches is accomplished by changing the duty ratios to D'_{AH}, D'_{BH} and D'_{CH}. In order to get the top group switches (1, 3, 5) gate pulses of the inverter from Fig. 5 in ΔADC and ΔEFC,

$$\frac{DC}{DF}=\frac{AD}{EF} \tag{9}$$

$$\frac{1}{t/2}=\frac{D_A}{\left(\frac{t}{2}-\frac{t_y}{2}\right)} \tag{10}$$

$$t_y=t\left(1-D_A\right) \tag{11}$$

From Fig. 5 in ΔAGH and ΔADC,

$$\frac{GH}{GA}=\frac{DA}{DC} \tag{12}$$

$$\frac{D'_{AH}}{\left(\frac{t}{2}-\frac{t_d}{2}-\frac{t_y}{2}\right)}=\frac{1}{t/2} \tag{13}$$

$$D'_{AH}=\frac{2}{t}\left(\frac{t}{2}-\frac{t_d}{2}-\frac{t_y}{2}\right) \tag{14}$$

Substituting from (11) in (14) we get,

$$D'_{AH}=\frac{2}{t}\left(\frac{t}{2}-\frac{t_d}{2}-\frac{t}{2}\left(1-D_A\right)\right) \tag{15}$$

$$\frac{1}{t/2}=\frac{D_A}{\left(\frac{t}{2}-\frac{t_y}{2}\right)} \tag{16}$$

$$D'_{AH}=D_A-\frac{t_d}{t} \tag{17}$$

$$D'_{AH}=D_A-t_d f_c \tag{18}$$

Similarly the required duty ratios for the other two phases D'_{BH} and D'_{CH} are generated for the required dead time and are given in (19) and (20).

$$D'_{BH}=D_B-t_d f_c \tag{19}$$

$$D'_{CH}=D_C-t_d f_c \tag{20}$$

The dead time insertion in lower switches is accomplished by changing the duty ratios to D'_{AL}, D'_{BL} and D'_{CL}. Similarly to get low gate pulses from Fig. 5 in ΔAKL and ΔADC,

$$\frac{KE}{KA}=\frac{DA}{DC} \tag{21}$$

$$\frac{D'_{AL}}{\left(\frac{t}{2}+\frac{t_d}{2}-\frac{t_y}{2}\right)}=\frac{1}{t/2} \tag{22}$$

$$D'_{AL}=\frac{2}{t}\left(\frac{t}{2}+\frac{t_d}{2}-\frac{t_y}{2}\right) \tag{23}$$

Substituting from (11) in (14) we get,

$$D'_{AL}=\frac{2}{t}\left(\frac{t}{2}+\frac{t_d}{2}-\frac{t}{2}\left(1-D_A\right)\right) \tag{24}$$

$$D'_{AL} = D_A + \frac{t_d}{t} \quad (25)$$

$$D'_{AL} = D_A + t_d f_c \quad (26)$$

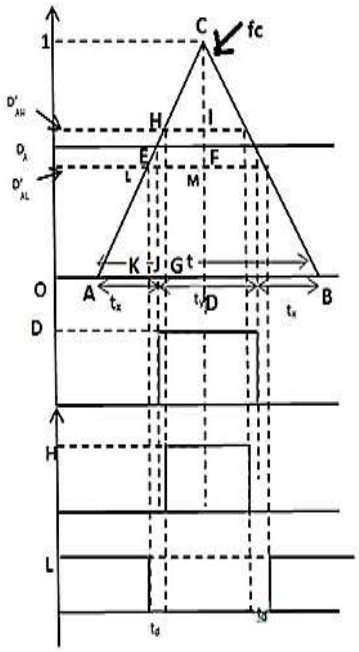

Fig. 4. High and Low Gate Pulses for Two-level Inverter

IV. RESULTS AND DISCUSSION

A. *Simulation Resuts*

The proposed algorithm is simulated using MATLAB simulink environment. Using conventional SVPWM for two-level inverter fed induction motor drive the steady performance of the drive is investigated at no-load. The measured parameters in terms of the line voltage THD, line current THD for conventional SVPWM is given in Table 1. The model developed in the matlab simulink environment can be loaded into the arm processor shown in Fig. 5. Fig. 6 gives the rotor speed, stator currents, and electromagnetic torque of induction motor using IDTSVPWM. simulated at no-load condition. Fig. 7 and 8 gives the harmonic spectrum of stator current and voltage THD's. Also with the modified IDTSVPWM algorithm the measured line voltage and stator current THD's are compared in Table 1.

B. *Hardware Results*

The experimental set-up for validating the proposed method is shown in Fig. 9. As the processor used is a high speed DSP processor it is even possible to further examine the performance of two-level inverter fed induction motor drive at different carrier frequencies and dead times. However it is observed from experimental set-up that the optimum performance of the drive is obtained at f_c=5 kHz and t_d= 4μs and m=0.866. The duty ratio using IDTSVPWM is shown in Fig. 10. The practical line voltage waveform is shown in Fig. 11. The practical stator current with IDTSVPWM is shown in Fig.12.

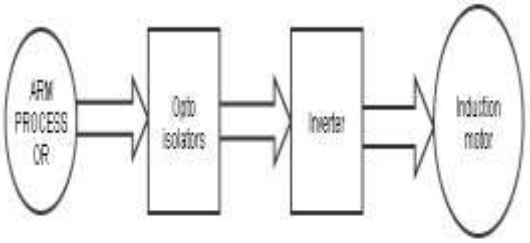

Fig. 5. Block diagram for hardware implementation

The output ports are configured for gate signals as outputs.The processor used is Discovery STM32F4.The outputs of the processor are given to opto isolators. MOSFETs are used in the inverter circuit since the switching frequency is very high. The MOSFET requires a gate to source voltage of 12 -18V to turn on, but the output of processor and opto isolators is only 5V. Hence a gate driver is used to turn on the MOSFET.

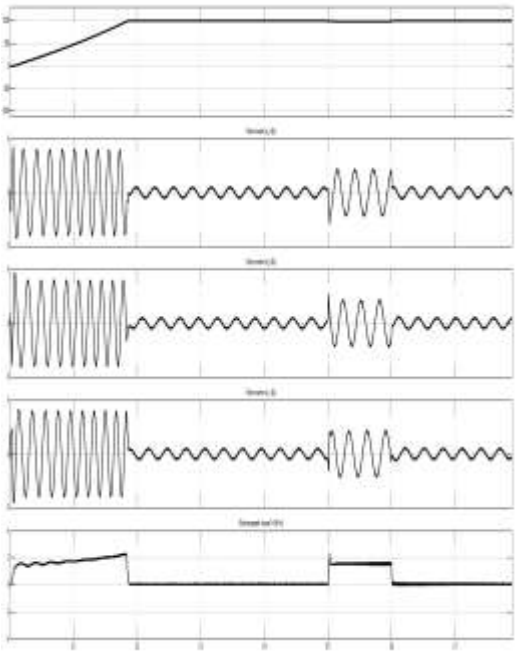

Fig. 6. Speed, Stator Current and Torque of Induction Motor

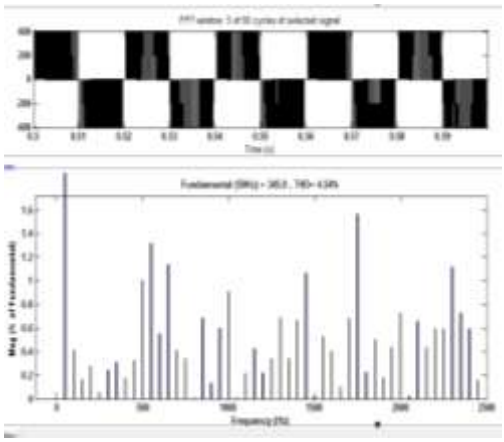

Fig. 7. Line Voltage THD and Harmonic Spectrum

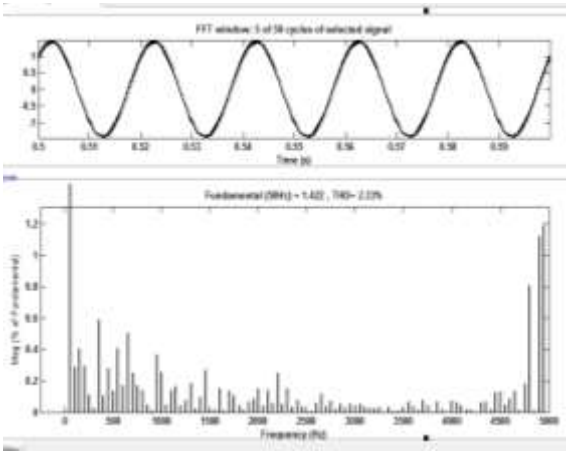

Fig. 8. Stator current THD and Harmonic Spectrum

TABLE I. MEASURED LINE VOLTAGE AND STATOR CURRENT THD'S

S.No.	Type of SVM	Line Voltage THD%	Stator Current THD%
1.	Conventional SVPWM	4.54	3.14
2.	Practical IDTSVPWM	5.573	2.568

Fig. 9. Connections of Experimental Set-Up

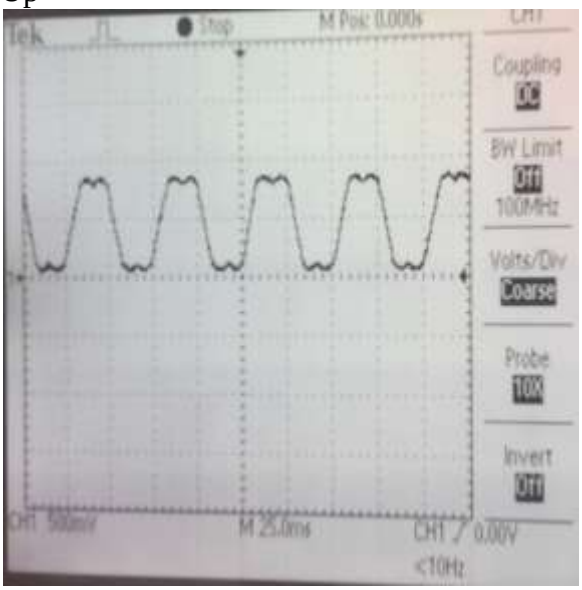

Fig. 10. Duty ratio for IDTSVPWM

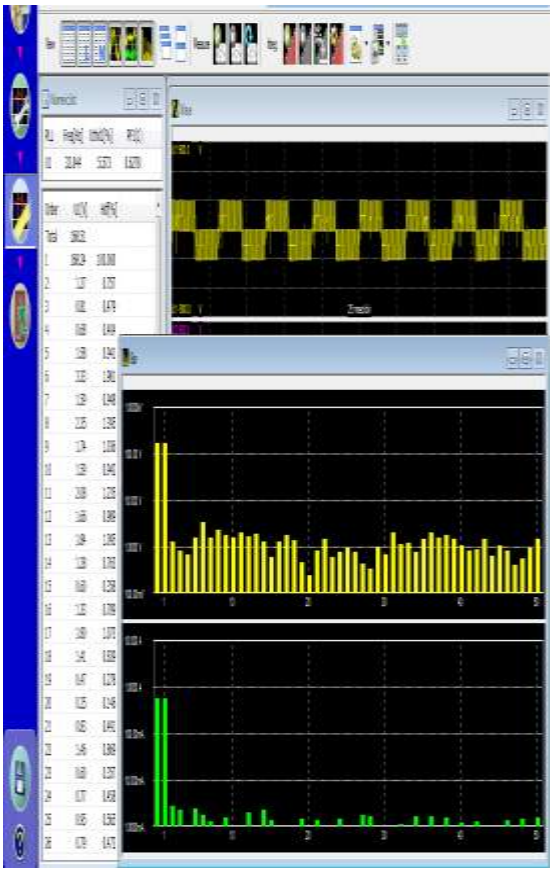

Fig. 11.Experiment based Line Voltages THD and Harmonic Spectrum

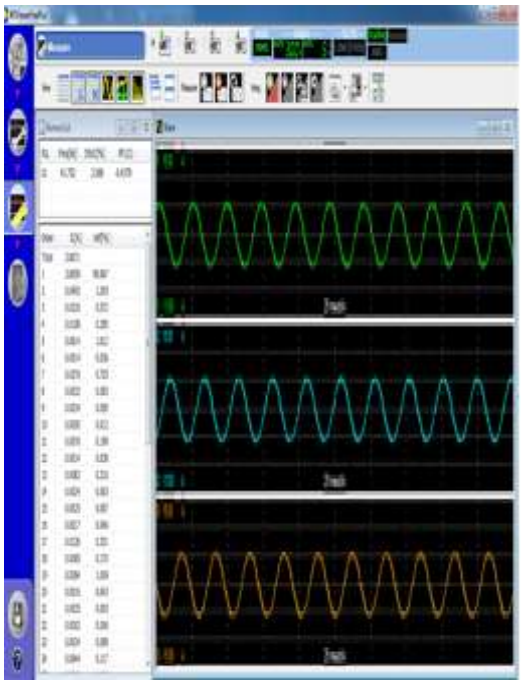

Fig. 12. Experiment based Line Currents THD and Harmonic Spectrum

V. CONCLUSIONS

An A new integrated dead-time space vector pulse width modulation (IDTSVPWM) technique to control a voltage source inverter (VSI) fed induction motor drive is presented using STM32F407 DSP processor. The main advantage of this method is that it eliminates the complexity in the inverter circuit by injecting dead time in the inverter from the obtained duty ratios.

APPENDIX

The ratings of the induction motor 400 Volts, 0.75 kW, 4-Pole, 1430 rpm. Induction motor parameters: R_s=12.71Ω, R_r^1 =9.92 Ω, L_s = L_r^1 = 0.03968H, L_m= 0.56238H, J= 0.002 Kg - m^2, F = 0.0005985 N-m-sec and inverter voltage V_{dc} = 200V. DC link capacitor 2700μF. MOSFETs used are IRFP460.

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