STUDY ON BUILT-IN-SELF-TEST (BIST) ENABLED UART USING VERILOG

LATHA DHULIPALLA
M.Tech (VLSI) Department of ECE
Priyadarshini Institute of Technology and Management.
Pulladigunta,Guntur, A.P.

YENDLURI KONDAIAH
Associate professor Department of ECE
Priyadarshini Institute of Technology and Management
Pulladigunta, Guntur, A.P.

ABSTRACT

Asynchronous serial communication is typically implemented by Universal Asynchronous Receiver Transmitter (UART), mostly used for low cost, low speed, short distance information switch between processor and peripherals. UART allows full duplex serial message link, and is used in data communication and control system. There is a need for realizing the UART function in a single or a very few chips. Further, design systems without full testability are open to the increased possibility of product failures and missed market opportunities. Also, it is necessary to ensure the data transfer is error proof. This project targets the introduction of Built-in self test (BIST) and Status register to UART. The basic idea is to reduce the switching activity among the test patterns at the most. In this approach, the single input change patterns generated by a counter and a gray code generator are Exclusive-ORed with the seed generated by the low power linear feedback shift register [LP-LFSR]. The 8-bit UART with status register and BIST module is coded in Verilog HDL and synthesized and simulated using Xilinx XST and ISim version 14.4 and realized on FPGA.

Keywords: - *BIST Architecture, UART Tx, UART Rx, LFSR, VLSI testing.*

I. INTRODUCTION:

The electronics industry has achieved a phenomenal growth over the last two Decades, mainly due to the rapid advances in integration technologies, large-scale systems design - in short, due to the advent of VLSI. The number of applications of integrated circuits in high-performance computing, telecommunications, and consumer Electronics has been rising steadily, and at a very fast pace. Typically, the required computational power (or, in other words, the intelligence) of these applications is the driving force for the fast development of this field. Gives an over view of the prominent trends in information technologies over the next few decades. The current leading-edge technologies (such as low bit-rate video and cellular communications) already provide the end-users a certain amount of processing power and portability. This trend is expected to continue, with very important implications on VLSI and systems design. One of the most important characteristics of information services is their increasing need for very high processing power and bandwidth (in order to handle real-time video, for example). The other important characteristic is that the information services tend to become more and more personalized (as opposed to collective services such as broadcasting), which means that the devices must be more intelligent to answer individual demands, and at the same time they must be portable to allow more flexibility/mobility.

Very-large-scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip. VLSI began in the 1970s when complex semiconductor and

communication technologies were being developed. The microprocessor is a VLSI device. The term is no longer as common as it once was, as chips have increased in complexity into the hundreds of millions of transistors.

II. BIST ARCHITECTURE

BIST architecture consists of a take a look at Pattern Generator (TPG), the circuit to be tested (CUT), some way to investigate the results (TRA), and some way to compress those results (BCU) and also LFSR for simplicity and handling. CUT could be designed as memory device architecture for testing the faults. The fault address can be detected and it could compare to the comparator for the analysis of the all relevant circuits.

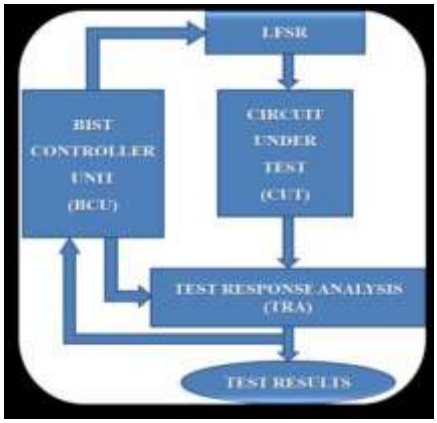

Figure 1: Block diagram of BIST architecture

The LFSR generates the feedback values from the each and every flip-flop for the new CUT architecture. The level of this recognition could be difficult to identify the fault and it could be having time consuming process. The process can be adoptable for the all authorized and the unauthorized data's. The BIST controller can be easily controlled as a device details for the novel architecture for the further details. The test response analysis could be considered for the UART transmitting and the receiving data's form the each bits. The test results can be detecting the fault address and then it consumes all the details as a database and identifies the fault address and shows the details. This could be as a process of simulation level waveform.

III. UART ARCHITECTURE

A universal asynchronous receiver/transmitter, abbreviated UART , is a computer hardware device that translates data between characters (usually bytes) in a computer and an asynchronous serial communication format that encapsulates those characters between start bits and stop bits.

The UART architecture contains the transmitter and the receiver. This could be contain and loads the buffer data for all the read and write operation. The data transfers through this serial communication to get the proper information about the outputs.

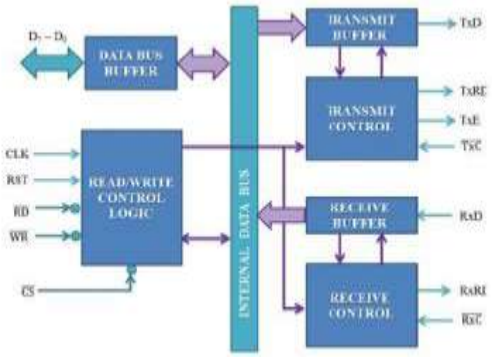

Figure 2: Block diagram of UART Architecture

UART COMMUNICATION

In UART communication, two UARTs communicate directly with each other. The transmitting UART converts parallel data from a controlling device like a CPU into serial form, transmits it in serial to the receiving UART, which then converts the serial data back into parallel data for the receiving device. Only two wires are needed to transmit data between two UARTs. Data flows from the Tx pin of the transmitting UART to the Rx pin of the receiving UART

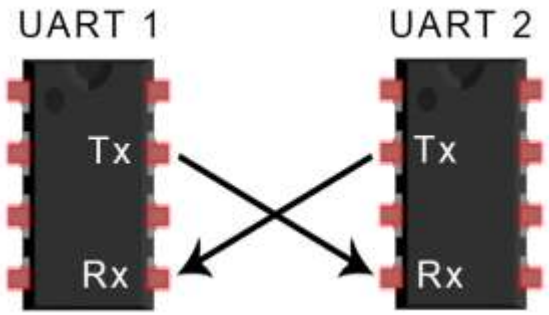

Figure 3: UART communiatiion

The universal asynchronous receiver/transmitter (UART) takes bytes of data and transmits the individual bits in a sequential fashion. At the destination, a second UART re-assembles the bits into complete bytes. Each UART contains a shift register, which is the fundamental method of conversion between serial and parallel forms. Serial transmission of digital information (bits) through a single wire or other medium is less costly than parallel transmission through multiple wires.

IV. SIMULATION RESULTS

The UART BIST architecture simulation can be done through the Xilinx ISE using VERILOG HDL. The data address bit verification can also to be done through this simulation and the waveform could be verified by using the MODELSIM.

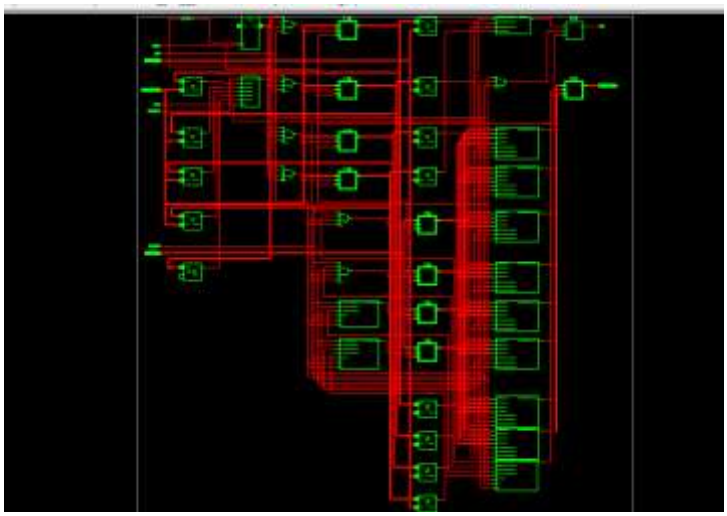

Figure 4: Architecture of UART

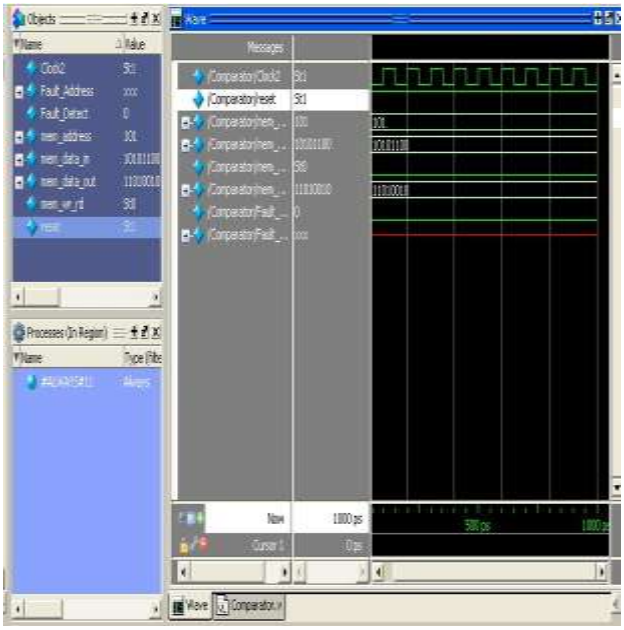

Figure 5: Waveform of UART architecture

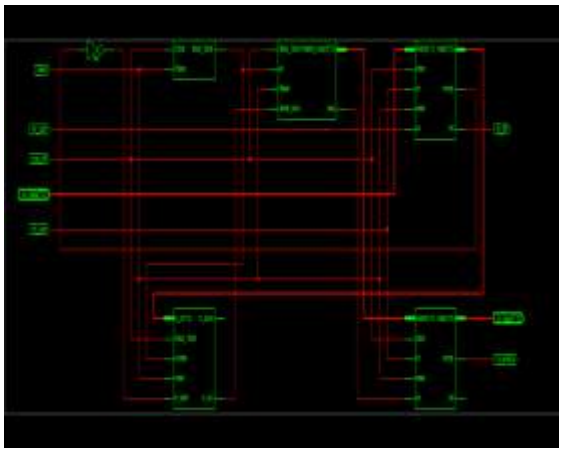

Figure5: Architecture of BIST

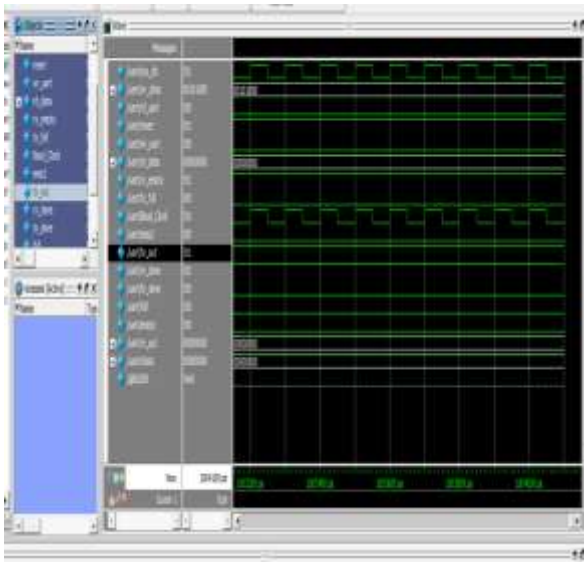

Figure 7: Waveform of BIST architecture

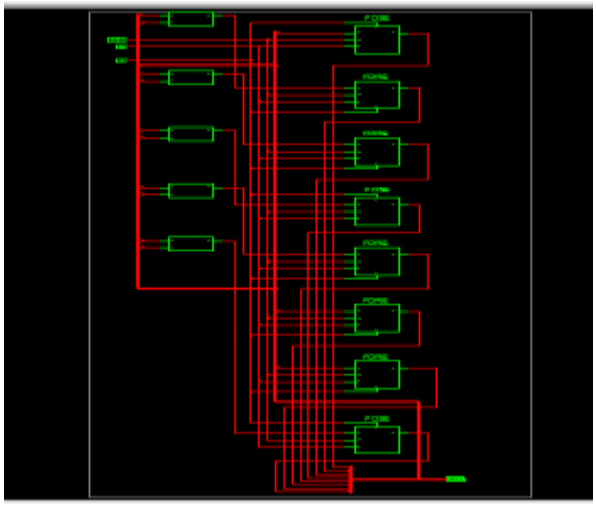

Figure 8: Architecture of LFSR

V.CONCLUSION

This papers presents the UART based BIST Architecture using VERILOG HDL. Most of the researchers have been used to implement this testing algorithm in VERILOG for stable, compact and reliable transmission. The structural details have been recognized and it can be integrated into the chip could be easier. The UART transmission could be relatively used in all the devices for the reliable transmission of data's from the structure where it could be converter and tested as a bit files generation. This design function can be adopted as a technical preserving data's for communication. The BIST controller as a device uses as an efficient bit generation for the chip implementation.

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