ANALYSIS OF THE PERFORMANCE AND RELIABILITY OF VLSI INTERCONNECTS

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Abstract
Transistor integration and downsizing were key to early semiconductor advancements, but connection constraints today drive performance. The industry has responded to this by implementing two major strategies: switching from aluminum/silicon dioxide (Al/SiO_2) to copper/low-k (Cu/low-k) interconnects systems and adding numerous metal line layers. Despite providing better electrical performance, copper interconnects have reliability issues include electromigration-induced deterioration, early via failures, and grain structure impacts. The length of on-chip interconnects has expanded dramatically due to technological scaling, which has prompted sophisticated integrated circuits to design with interconnects in mind. While low-k dielectrics seek to minimize RC latency, power consumption, and crosstalk, higher current densities amplify Joule heating. Advanced interconnect performance analysis is required because standard modeling often fails to properly forecast bandwidth and latency in complex System-on-Chip (SoC) designs. In order to maintain the scalability and functionality of next semiconductor technologies, this research looks at the performance and dependability of Cu-based interconnects.

Keywords: *Analysis, Performance, Reliability of VLSI, Semiconductor interconnects, RC delay.*

INTRODUCTION
Since transistors and interconnections make up an integrated circuit, the dependability of these components determines the reliability of the integrated circuit as a whole. If nothing is done for the interconnection design and procedure, the reliability of the interconnection will deteriorate dramatically as the interconnect line width in VLSI decreases, making the reliability analysis of interconnections more important. Actually, research has shown that as technological nodes have improved, the failure rate linked to interconnect failure in VLSI is rising sharply in current day and age.

The NBTI, PBTI, and TDDB are the three failure modes that are common in today's VLSI interconnection system. The Interconnect Chapter of the 2013 ITRS roadmap also explains this. Current density is no longer the only factor affecting interconnection reliability; temperature distributions and the resulting thermo-mechanical stress distribution are also significant influencing factors that need to be taken into account, especially with the growing complexity of the interconnection system and its 3D nature in actual implementation, along with the use of low-k dielectric. Because of this, it is challenging to analyze interconnection dependability. It is possible to conduct reliability tests like the electromigration, stress-induced voiding, and time-dependent dielectric breakdown (TDDB) tests, but they can take too long to complete and it can be challenging to pinpoint the underlying mechanisms interacting during the degradation process. FEM for VLSI connectivity based on physics is a complicated topic. Even if there has been a lot of development recently, there is still a lot of room for study to enhance the modeling capabilities.

OBJECTIVES
1. Examine how interconnect material characteristics affect the dependability and performance of VLSIs.
2. Examine crosstalk noise, power consumption, and delay in various scenarios.

REVIEW OF LITERATURE

Kazushige Toriyama et al. (2012)

In this article, we investigated the die thickness and the fine pitch (50um) flip chip interconnections with different bump configurations. We analyzed the three different die thicknesses (100um, 300um, and 75um) and the three kinds of solder-capped metal (Cu, Cu-Ni, and Ni) pillar bumps. The thermal mechanical load on the solder junction and the metal pillar root was initially examined using FEM modeling. The outcome demonstrated that the stress on the pillar root on the Ni pillar bump was greater than that on the Cu pillar bump, and that reducing the die thickness decreased the stress on the solder junction and the pillar root.

Pavel Livshits et al. (2011)

This study's findings show that the MOSFETs' dynamic power consumption increases and their wearout process from hot carrier injection (HCI) accelerates as resistive losses increase. Additionally, it was shown that in situations where these MOSFETs are loaded directly by the interconnection line, the deterioration of MOSFETs (attached to the far end of the line) due to HCI is also hastened, and the electromigration and Joule heating of this line are intensified (regardless of the amount of losses in the line). As a result, interconnect resistive losses are a significant reliability concern that has to be included in the relevant reliability models.

Abhishek Pan et al. (2009)

Device reliability issues that result in partial system failure or shutdown are to blame for a growing number of hardware failures. In this research, we provide a method for increasing a homogeneous chip multiprocessor's (CMP) stability while simultaneously increasing manufacturing yield. Using this service may increase yield and dependability, but there may be some performance loss.

Hong Li et al. (2008)

We offer the first compact equivalent circuit model of MWCNTs and compare the performance of MWCNT interconnects with that of conventional Cu interconnects. According to research, MWCNT interconnects can achieve lower signal delays than Cu interconnects at the intermediate and global levels. However, because MWCNTs are simpler to fabricate and require less attention to density control, they may be more appealing for immediate use as horizontal wires in VLSI, including local, intermediate, and global level interconnects.

Fred Chen et al. (2007)

The necessity to assess the effects of new interconnects technologies, including carbon nanotubes (CNTs), in relation to system applications is the focus of this paper's study. The interlayer dielectric (ILD) stack-up and wire diameters are rescaled using this technique for various combinations of copper and carbon nanotube (CNT) interconnects and vias. The stack-ups are then analyzed in an on-chip network application. For a power-constrained on-chip network application, the results of adjusting the ILD and wire sizing for a conservative estimate assuming a CNT bundle with 1/3 contacted metallic CNTs demonstrated a 50% increase in total system throughput and a 30% improvement in delay and energy over copper at the 22 nm node.

Kenichi Okada et al. (2006)

This study assesses the viability of 45nm CMOS on-chip transmission line connectivity. Global interconnects have a tendency to have a significant impact on circuit performance, and as process technology becomes smaller, global interconnect power and latency grow. There is a proposal for an on-chip transmission line that can help with the lengthy RC interconnects' high power consumption and latency.

Only one connector has had the improvement assessed. This study uses the measurement findings at 180nm technology to analyze the overall circuit power decrease for 45nm technology. For instance, on a circuit intended for a 45nm process, the power consumption of global interconnects is enhanced by 6.6%. The

transmission line uses less power than the RC line in lengthy interconnect and it can transmit signals more quickly than an RC interconnects. The RC interconnects are replaced by the transmission-line interconnect, which is made up of a driver, a differential transmission line, and a receiver.

METHODOLOGY

Device densities and speeds have significantly risen due to advancements in VLSI technology. Device connectivity, which uses polysilicon or aluminum wires, has not altered all that much, however. Therefore, the power consumption, delay time, and surface areas needed by present connection technologies often restrict the performance of modern VLSI systems [29].

Finding the dependability of an inverter circuit and two CMOS gates—a combination of two inverters coupled with an RC model as an interconnect structure—using the cadence virtuoso tool at gpdk 45 nm technology is the aim of this study. Hot-carrier injection, negative biasing temperature instability, positive biasing temperature instability, and the modest influence of time-dependent gate oxide breakdown are the main factors that determine reliability in electronic circuits. This inverter applies a capacitive load at the output terminal while having no load impact at the output terminal. The process of reliability analysis involves evaluating output voltage, power, and delay after a predetermined amount of time.

We now examine the Two CMOS Gate example (a combination of two inverters connected by an RC model) in order to compare the impact of electrical interconnects. The diagram that follows shows two CMOS gates.

Using the pch and nch model libraries, respectively, the above figure displays the schematic of a two CMOS gate circuit with two PMOS of width 2.5 um and length 45 nm and two NMOS of width 1 um and length 45 nm. A 1.1 V pulsing signal with rise and fall times of 10 ps, pulse width of 10 ns, and period of 20 ns is used to apply the input. The circuit operates at VDC 1.1 V utilizing BSIM4 model files, which covers the physical effects of MOSFETs for 40 ns in the sub-100 nm region. An RC model makes up the electrical connection between the two inverters.

The three capacitances are the line capacitance CL, the output capacitance of the CMOS driving gate Co, and the input capacitances of the CMOS driving gate Cin. Cin comprises the two transistors' gate capacitances that jeopardize the receiving gate.

RESULT AND DISCUSSIONS

Analysis of Electrical Interconnection of Two CMOS Gate Schematic

The transient analysis is analyzed for 100 ns, and Vin Vs Vout is calculated with calculating the power of each component used in the circuit.

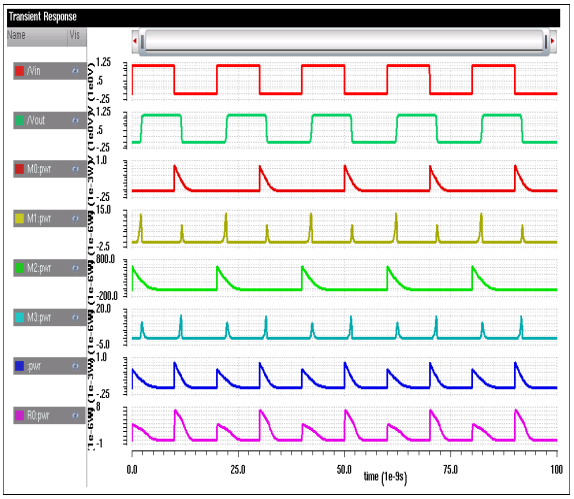

Fig 1:- Transient response of Two CMOS Gate (Vin, Vout, power consumed by Mo, M1, M2, M3, Power of the circuit & power consumed by of resistance)

Table 1:- Values obtained in transient analysis of Two CMOS Gate for duration of 0 to 100 ns.

Max Value of Vin	1.1 V	Min Power of PMOS-1	12.09E-18 W

Min Value of Vin	0 V	Max Power of NMOS-1	13.24E-6 W
Avg Value of Vin	550.6E-3 V	Min Power of NMOS-1	333.4E-18 W
Max Value of Vout	1.1 V	Max Power of PMOS-2	610.1E-6 W
Min Value of Vout	-149.4E-6 V	Min Power of PMOS-2	449.9E-18 W
Avg Value of Vout	519.5E-3 V	Max Power of NMOS-2	15.9E-6 W
Max Power of Circuit	837.6E-6 W	Min Power of NMOS-2	2.454E-18 W
Min Power of Circuit	114.0E-12 W	Max Power of R0	7.150E-6
Avg Power of Circuit	123.3E-6 W	Min Power of R0	469.2E-21 W
Max Power of PMOS-1	837.5E-6 W		

Further DC analysis is done and the corresponding values of Vin, Vout and power is calculated. DC analysis is analysed in the range from -5 V to 5V.

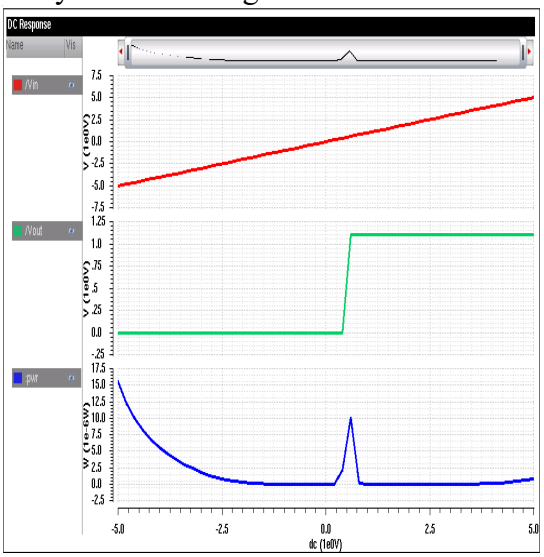

Fig 2:- DC response of Two CMOS Gate schematic (Vin, Vout & Power of the circuit).

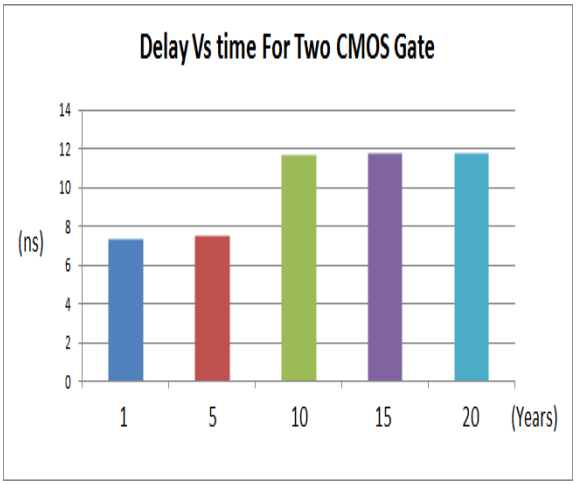

Fig 3:- Reliability in terms of delay vs. time for Two CMOS Gate.

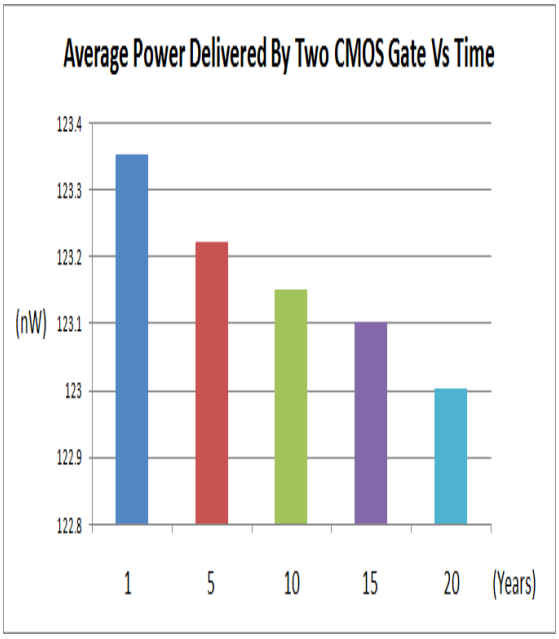

Fig 4:- Reliability analysis in terms of average power delivered vs. time for Two CMOS Gate

This leads to a study of the inverter's and two CMOS gates' performance and dependability. It has been shown that the impacts of HCI, NBTI, PBTI, and TDDB phenomena cause their performance to deteriorate with time. The average power that the circuit delivers is the sole way to do reliability analysis on an inverter. On the other hand, the average power provided by the circuit across various time intervals and the delay between input-output voltage are used to analyze the dependability of two CMOS gates,

respectively. Transistor level circuit modeling is the foundation for all reliability simulation tools created to date. Therefore, it is necessary to create a higher level dependability simulator that considers.

CONCLUSION

In order to determine the circuit is transient analysis, ac response, power delivered during the transient response, noise response, and reliability in terms of delay and power delivered, as well as the effects of interconnects taking into account RC model interconnect, a schematic representation of an inverter and two CMOS gates are also simulated on CADENCE Virtuoso at 45 nm technology, respectively. In order to determine the transient analysis, power delivered by the circuit, noise response, reliability in terms of delay, power delivered by the circuit, operating frequency of the circuit, operating frequency of the PMOS & NMOS devices, and the effects of interconnects, the schematic representations of the Transmission Line Circuit for Interconnects, transmission line as a set of two parallel wires, and Thirteen Stages CMOS Ring Oscillator are also simulated on CADENCE Virtuoso at 45 nm technology, respectively.

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