

## AN OVERVIEW OF VLSI FOR MEDICAL APPLICATIONS

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### Abstract

*With growing expenditures and an aging population, health care is getting more and more costly in the modern period, yet the government is unable to provide the necessary funds. Patients are experiencing trauma as a result of this issue and finding it difficult to get medical care. Wireless communication in this situation lowers expenses and patient suffering. The very large scale integration (VLSI) principle, which is appropriate for biomedical applications, may be used to create this wireless system. In neurology, the use of VLSI techniques aids in circuit size reduction, area reduction, and speed enhancement. The design of a medical implant communication system (MICS) receiver for biomedical applications, the field programmable gate array (FPGA) implementation of neural networks, the neuro-fuzzy system, the implementation of neural networks in analog hardware, and the implementation of neural networks in digital networks are discussed in this review. These methods and techniques' benefits and shortcomings are also discussed.*

**Keywords:** FPGA, neural networks, biomedicine, and VLSI

### Introduction

With a rising population, medical treatment has become more expensive, and the general public is unable to pay for the services due to high costs. In order to eliminate this load, new technologies are being used. Medical services using wireless technology may be more affordable, less traumatic for patients, and easier for patients to navigate. Wireless technology has advanced with new aspects and begun employing RF circuitry components, RF transceiver, IF mixer, etc. to lessen the patients' suffering when using

any medical services in daily life. This is primarily to preserve the low power consumption in the medical area. To improve short-range medical communications between implanted medical devices and outside equipment, the Medical Implant Communication System (MICS) was developed [1]. In order to diagnose and track biomedical signals between low power implanted medical devices and other equipment, the MICS band is employed as a short-range wireless connection. The Federal Communications Commission (FCC) has studied the frequency range between 402 MHz and 405 MHz for MICS applications [2, 3]. The MICS band receiver system seeks to be completely integrated, low power, compact, and affordable.

The medical specialty of neurology focuses on the diagnosis and treatment of conditions and illnesses affecting the nervous system and brain. Patients with epilepsy, traumatic brain damage, movement abnormalities, and other neurological conditions are also treated by neurologists in addition to stroke victims. A parallel algorithm is an artificial neural network (ANN). As a result, it may be used in parallel VLSI implementations where the circuits or designs can carry out their activities concurrently [5-7]. Parallelism, straightforward operations, and high computing load are the main

factors driving the increasing popularity of VLSI implementation of artificial neural networks. Analog implementations think ANN is only suitable for straightforward processes. Since the operations are straightforward, analog cells with few transistors may effectively implement them [8]. Using analog calculations, ANN algorithms' accuracy is variable and constrained. This kind of procedure involves a high number of parallel operations per second (HPS). Parallelism is not possible in digital implementations since there are only a finite number of digital cells. Digital implementations are less favorable than analog ones in terms of HPS. Analog circuits are often restricted in their accuracy, but digital circuits need an awareness of the trade-off between precision and complexity. The majority of applications using sensors and signal processing will be based on application-dependent systems, where the application will be integrated on one or a few components. This is the basis for our assumption that neural network VLSI implementation would gradually gain popularity in the market today [9].

The following is a plan for the paper. Sect. 2 provides a summary of the literature review on VLSI implementation in biological applications. Sect. 3 reports a comparison of earlier studies with the related outcomes. Sect. 4 completes it at the end.

### **Literature Review**

For feed forward neural network VLSI operation, Shinde, J. R. et al. [10] proposed a most advantageous multi-objective optimization approach to ensure that it can be either area/power/speed efficient simultaneously. In order to enhance space, power, and speed while maintaining high accuracy and dynamic

range for neural network hardware design, a step-by-step ideal multi objective technique is adopted. Regarding data representation, analog vs digital neural networks, and multiplier units, it has several implementation design flaws. The multi-objective optimization for ANN has been accomplished using a digital neural network, floating point arithmetic, and an array multiplier, although there are significant limitations. Without interfering with the operation of the circuits and filter module, it has been possible to design a digital FIR filter on a VLSI chip while simultaneously optimizing its area, power, and speed. Synopsis Design Compiler is used to create designs for 45 nm and 90 nm processes [8, 11].

In their study [12], Omondi, A. R. et al. concentrated on the effective execution of ANN calculations on massively parallel computing systems built in FPGA. The bit-serial processor array used to build the computer was run using FPGA circuits. The method is now more scalable in terms of size and clock speed. Several VLSI generations have had problems, however the FPGA implementation of neural networks has been improved with current technology to fulfill expectations for current trends. Programmable systems have versatility thanks to FPGA. [5, 13] describe a hardware neural network implementation employing FPGA chips with cheap cost, lower error, best outcome, and improving efficiency. The stochastic method has produced the greatest results for the hardware implementation of neural networks that uses little power and little space. Energy consumption reduction and improved performance have been examined using quasi-synchronous technology [9].

The concept of calculating in the brain and

how it should be planned on future computer systems was put out by Arbib, M. A. [14]. Artificial intelligence (AI), neurology, artificial neural networks, and control theory are the key topics. Supportive computation, schemas, synchronized control programs, action-oriented perception, various brain levels, and perception-oriented action, where schema is the major goal, are the important concepts in this work. As a result of its integration of neural networks and other approaches, the significance of the link between action and perception, and its unique approach to natural language processing, it is relevant to the distribution computing at different levels of description. It also provides information about artificial intelligence with an emphasis on modern applications that use ANNs and AI. The fuzzy controller approach is used to enhance the interpretation of the data.

The analog hardware implementation of neural networks was discussed by Draghici, S. [15]. The terminology created using these requirements is shown. There have been many categories of generic neural network operations proposed. Researchers, businesses, and quick delays have always found the analog form of neural networks to be outstanding. Other real-world uses for analog circuits running neural networks include nuclear physics, intelligent control, tracking, and target identification. Design and coding processes use VLSI-friendly algorithms.

The comparison of analog and digital types of neural networks was proposed by Kakkar, V. [16]. It demonstrates which implementation style is best for different applications. This research bases its findings on layered feed forward neural networks and restricts its neural network

operations to pattern recognition. Classification issues are a good fit for digital neural networks. They outperform analog types in areas like resilience, drift, noise, and logic description. They also load digital weights quickly, don't need feedback, and can adapt to new processes and architectural designs. Afterwards it is discovered that an analog neural network performs better for classification problems with minimal power consumption.

According to Morgan, N. et al. [17], parallelism is a kind of method utilized by ANN in signal processing and pattern recognition. For digital ANN design, a collection of library cells tailored to ANNs and a CAD interface are utilized. The definition of a new silicon productivity metric for ANNs. It has assessed the current and upcoming circuit implementations of popular ANN algorithms to highlight the relative efficacy of silicon utilization in the context of the specific application. According to the conclusion, digital implementation is more adaptable and efficient than analog operations.

For the purpose of designing bespoke chips, Lotric, U. et al. [18] investigated a large range of internal parallelism of neural networks. With the use of FPGA technology, this study focuses on the actual digital design of a hardware neural network. Moreover, it seeks to propose a source and include a feed-forward neural network with on-chip learning capabilities. To produce a better design, neural network processing must be carried out in parallel since it involves a lot of multiplication. Since there aren't enough chips, fixed point math is employed. Hardware neural networks are constructed with the use of iterative logarithmic multipliers, which employ several layers of rectification

circuits to get a result to the level of subjective accuracy. Ultimately, neural networks develop into a power-saving, adaptive model.

According to Madhumitha, G. B. et al. [19], ANN is the ideal solution for complicated biological systems that need adoption and learning. Analog and digital operations are used to construct an ANN. In order to solve the issues with weight accuracy, device mismatch, and precision, this study proposes the development of an ANN with low power and low area, comparable to the biological arrangement in analog domain. This neural network design makes use of the back propagation method. Circuits that execute arithmetic operations and neural networks are implemented using CMOS 180 nm technology. Neural networks are used to do signal compression. Here, neural networks may be implemented using VLSI using both analog and digital signals.

The knowledge-based neural network model with hyperbolic tangent function was suggested by Suganya, A. [20] using the hashing approach. In Xilinx 12.1, the VHDL programming language is utilized for coding and simulation purposes. In the VLSI operation of ANN, it decreases the number of multiplications, area, power, latency, cost, and computation.

An summary of earlier work in neuromorphic computing was published by Schuman, C. D. et al. [21]. In the past, neuromorphic and neural network hardware has employed a variety of neurons, synapse, and network models. It is uncertain if a large variety of models will be integrated into one in the future since each model has its own advantages and disadvantages. From feed forward neural networks to biological neural networks, neuromorphic computing is all

around us. With the use of learning techniques like the back propagation algorithm and supervised learning, neural networks serve as a software model that aids in the discovery of incorrect calculations made by the human brain and anticipates one of the yearly export air cargo commands [22].

The design of neurons, extended range loads, and digital networks were covered by Ranade, R. et al. [23]. The energy function for the multiplication function is constructed with the aid of ANN. Due to its parallel computations, ANN-related digital functions like multipliers and adders are beneficial. In [24], the perception of ANN is utilized to create a binary digital multiplier, and the multiplier takes into account synchronous, parallelism, and fast information processing speed as ANN compensation.

According to Kung, S. Y. et al. [25], neural networks are crucial for multimedia features such effective auditory information visualizations, classification and detection methods, signal mixing, and multimodal conversion and synchronization. Also presented is the adaptive neural network technology, which provides a consistent resolution for a variety of multimedia applications. It is obvious that working on these networks will present space constraint issues.

By focusing on content integration, incorporating with the human ear, and integrating with other media systems, multimedia may strengthen its position and influence.

According to Awodele, O. et al. [26], neural networks have advanced through time and have significantly improved a number of disciplines. Its goal is to examine neural networks and emerging applications in engineering, focusing

mostly on controllers. The requirements for neural networks, their training, and crucial methods for neural network construction are reviewed. In the current world, concerns mostly revolve around difficulties like neural network scalability, testing, verification, and integration. It is advised that intelligence systems undergo the same testing and verification processes that people undertake.

Although the experimental work was time-consuming and expensive, Hayati, M. et al. [27] provided a genuine convection heat transfer simulation from an appropriate isothermal horizontal elliptic tube based on ANN. The tube axis ratio, wall spacing, Rayleigh number, and average Nusselt number have all been employed as inputs and outputs, respectively. For calculating the free convection heat transfer coefficient, the multi layer feed forward network approach is employed to maximize the potential of artificial intelligence principles. To effectively estimate the average Nusselt number, a neural network is constructed.

Al-Allaf, O. N. A. [28] talks about face detection as one of the most related application of biometric, pattern recognition and image processing by the use of ANN. Different structural design, concepts, database for testing images, performance measuring of face recognition has been used. In future, face detection structure might be based on back propagation neural network with numerous hidden layers.

Egwoh, A. Y. et al. [29] shown that traditional algorithm approaches can't solve today's problems. Neuro-fuzzy

systems can tackle any issue and are becoming more popular. It discusses neuro-fuzzy uses in agriculture and other fields. Fuzzy logic is employed in robotics, engineering, and physics. This word is influencing medical science, engineering, and homes. They explained fuzzy logic and its modern applications. Fuzzification, inference, and defuzzification comprise fuzzy logic. Fuzzy logic helped math, chemistry, robotics, engineering, and medicine.

Jothi, M. et al. [30] used diabetes as a biological science healthcare problem. Diabetes causes epilepsy. It involves abnormal brain nerve cell activity. Diabetic epilepsy risk classification uses consistent fuzzy model. Two input rule technique inspects heterogeneous and homogeneous fuzzy systems. Fuzzy system is recommended for SRIM. FPGA examined the single and two rule approaches for cerebral blood flow level. FPGA synthesizes after Matlab testing and VHDL simulation. Quality and performance were sought to enhance the fuzzy classifier. Ultimately, FPGA and Matlab findings show comparable VLSI system average area and performance.

**Results and Comparison**

Neural network research is contrasted here. Several technologies confirmed the work's parameters. See specific works' difficulties and outcomes. Table 1 compares VLSI neural network systems. Ultimately, VLSI and wireless technologies will be employed to build a full neural network with minimal cost, power, and area.

**Table 1. Comparison of various VLSI implementation based neural network systems**

Refs.	Parameters	Implementation type	Issues	Output	Tools/Technology used
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[10]	Area, power, speed	Multi objective method	Data representation, analog vs digital and multiplier unit	Low area, low power and low speed multi-objective optimization ANN	MATLAB, VHDL
[12]	Clock speed, time	FPGA	Different generations of VLSI	Increase in scalability	VLSI
[14]	Brain calculations, action and perception	Neural schemas, ANN computations	Pattern recognition, different neural levels	Different neural schemas, action and perception w.r.t. natural language processing	Natural language processing
[15]	Analog hardware, neural networks	Analog type	Classification problems	Neural network implemented successfully	VLSI
[16]	Weight accuracy, drift, noise	Analog vs digital	Classification problems	NA	NA
[17]	Silicon productivity	Digital networks	Problems faced in analog type of implementation	Robust and flexible neural networks	Digital VLSI, CAD, ANN specific libraries
[18]	Speed, power, chip design	Hardware neural network, fixed point arithmetic	Multiplication circuit taking lot of resources and time	Adaptive and power efficient neural network	FPGA
[19]	Area, power, speed, signal compression	Analog type	Classification problems	Effective neural network and also applicable for digital operations	Analog VLSI
[20]	Area, power, delay, cost	Hyperbolic tangent function, hashing trick	NA	Weighted neuron net	VHDL, Xilinx 12.1
[21]	Neurons, synapses, network models	Hardware implementation	NA	Study of neuromorphic and neural network	NA

Refs.	Parameters	Implementation type	Issues	Output	Tools/Technology used
				hardware	
[23]	Energy function	ANN parallelism computations	NA	Design of energy function for multiplication	VLSI
[25]	Neural networks, multimedia applications	Statistical and parameter estimation techniques	Space limitation issues	Human communication with machines, audio/visual, pattern recognition	Intelligent multimedia processing technology
[26]	Neural networks, controls	NA	Scalability, testing and integration issues	NA	VLSI
[27]	Convection heat transfer coefficient	Multi-layer feedback network, back propagation	Time consuming and expensive	Average Nusselt number with low error	Horizontal elliptic tube method
[28]	Face detection	ANN	Lack of determination of face recognition	Partial Face detection system	Computer and information technology
[29]	Fuzzy logic	Neuro-fuzzy approach	NA	NA	NA
[30]	Fuzzy classifier, CBF, EEG	FPGA, fuzzy method and SRIM fuzzy system	Classification problems	VLSI fuzzy classifier	VHDL, MATLAB

### Conclusion

Biomedical systems need VLSI neural networks with minimal cost, power, and area. Biomedical monitoring, diagnosis, and control need MICS receivers with superior RF circuitry. Analog implementations are better than digital ones, while digital ones are more versatile, smaller, and faster. The literature review and comparison table will aid ongoing study in this field.

### References

- 1) Iniewski, K.: *VLSI Circuits for Biomedical Applications*. Artech House, Norwood (2008)
- 2) Hsu, C.M., Lee, C.M., Yo, T.C., et al.: *The low power MICS band biotelemetry architecture and its LNA design for implantable applications*. In: *Proceedings IEEE Asian Solid-State Circuits Conference, Hangzhou, China, pp. 435–438 (2006)*
- 3) Yuce, M.R., Ng, S.W.P., Myo, N.L., et al.: *A MICS band wireless body sensor network*. In: *Proceedings IEEE Wireless Communications and Networking Conference, Kowloon, China, pp. 2475–2480 (2007)*

- 4) Chang, C.H., Gong, C.S.A., Liou, J.C., et al.: A 260- $\mu$ W down-conversion demodulator for MICS-band receiver. *J. Circuits Syst. Comput.* 26(2), 1750027:1–1750027:10 (2017). <https://doi.org/10.1142/s021812661750027x>
- 5) Zaghar, D.R.: Reduction of the error in the hardware neural network. *Al-Khwarizmi Eng. J.* 3(2), 1–7 (2007)
- 6) Kumar, K., Thakur, G.S.M.: Advanced applications of neural networks and artificial intelligence. *Int. J. Inf. Technol. Comput. Sci.* 6, 57–68 (2012). <https://doi.org/10.5815/ijitcs.2012.06.08>
- 7) Chasta, N., Chouhan, S., Kumar, Y.: Analog VLSI implementation of neural network architecture for signal processing. *Int. J. VLSI Des. Commun. Syst. (VLSICS)* 3(2), 243–259 (2012). <https://doi.org/10.5121/vlsic.2012.3220>
- 8) Shinde, J.R., Salankar, S.: VLSI implementation of neural network. *Curr. Trends Technol. Sci.* 4(3), 515–524 (2015)
- 9) Ardakani, A., Primeau, L., Onizawa, F.N., Hanyu, T., Gross, W.J.: VLSI implementation of deep neural networks using integral stochastic computing. In: *Proceedings of 9th International Symposium Turbo Codes Iterative Information Processing (ISTC)*, pp. 216–220 (2016)
- 10) Shinde, J.R., Salankar, S.: Multi-objective optimization for VLSI circuits. In: *IEEE International Conference on Computational Intelligence & Communication Networks*, Kolkata, India (2014)
- 11) Shinde, J.R., Salankar, S.: Optimal multi-objective approach for VLSI implementation of digital FIR filters. *Int. J. Eng. Res. Technol. (IJERT)* 3(2), 2470–2474 (2014)
- 12) Omondi, A.R., Rajapakse, J.C.: *FPGA implementation of neural networks*, pp. 3–6. Springer (2006)
- 13) Sahin, S., Becerikli, Y., Yazici, S.: *Neural networks implementation in hardware using FPGAs*. LNCS, vol. 4234, p. 1105. Springer, Heidelberg (2006)
- 14) Arbib, M.A.: *The Metaphorical Brain: An Introduction to Cybernetics as Artificial Intelligence and Brain Theory*. Wiley, New York (1972)
- 15) Draghici, S.: Neural networks in analog hardware-design and implementation issues. *Int. J. Neural Syst.* 10(1), 19–42 (2000)
- 16) Kakkar, V.: Comparative study on analog and digital neural networks. *Int. J. Comput. Sci. Netw. Secur.* 9(7), 14–21 (2009)
- 17) Morgan, N., Asanovic, K., Kingsbury, B., Wawrzynek, J.: *Developments in digital VLSI design for artificial neural networks*. Technical report TR-90-065
- 18) Lotric, U., Bulic, P.: Applicability of approximate multipliers in hardware neural networks. *Neurocomputing* 96, 57–75 (2012). <https://doi.org/10.1016/j.neucom.2011.09.039>
- 19) Madhumitha, G.B., Devadiga, V.: Analog VLSI implementation of artificial neural network. *Int. J. Innov. Res. Comput. Commun. Eng.* 3(5), 72–80 (2015)
- 20) Suganya, A., Sakubar, S.J.: An priority based weighted neuron net VLSI implementation. In: *International Conference on Advanced Communication, Control & Computing, Ramanathapuram, India*, pp. 285–289 (2016)
- 21) Schuman, C.D., Potok, T.E., Patton, R.M., Birdwell, J.D., et al.: A survey of neuromorphic computing and neural networks in hardware. *Neural Evol. Comput.* 1–88 (2017)
- 22) Sivanandam, S.N., Sumathi, S., Deepa, S.N.: *Introduction to Neural Networks Using Matlab 6.0*, pp. 1–26. Tata McGraw-Hill, New Delhi (2006)
- 23) Ranade, R., Bhandari, S., Chandorkar, A.N.: VLSI implementation of artificial neural network based digital multiplier and adder. In: *Proceedings of the IEEE International Conference on VLSI Design, Bangalore, India*, pp. 318–319 (1996)
- 24) Biederman, D.C., Ososanya, E.T.: Design of a neural network-based digital multiplier. In: *Proceedings of the Twenty-Ninth South-Eastern Symposium on System Theory, Cookeville, TN*, pp. 320–326 (1997)
- 25) Kung, S.Y., Hwang, J.N.: *Neural networks for intelligent multimedia processing*. *Proc. IEEE* 86(6), 1244–1272 (1998)
- 26) Awodele, O., Jegede, O.: *Neural networks and its application in engineering*. In: *Proceedings of Informing Science & IT Education Conference*, pp. 83–95 (2009). <https://doi.org/10.28945/3317>
- 27) Hayati, M., et al.: Application of artificial neural networks for prediction of natural convection heat transfer from a confined horizontal elliptic tube. *World Acad. Sci. Eng. Technol.* 28, 269–274 (2007)
- 28) Al-Allaf, O.N.A.: Review of face detection systems based artificial neural networks algorithms. *Int. J. Multimed. Appl.* 6(1), 1–16 (2014)
- 29) Egwoh, A.Y., Onibere, E.M., Odion, P.O.:





*Application of neuro-fuzzy system: a literature review. Int. J. Comput. Sci. Netw. Secur. 18(12), 1–6 (2018)*

32) *Jothi, M., Balamurugan, N.B., Harikumar, R.: Design and implementation of VLSI fuzzy classifier for biomedical application. Int. J. Innov. Res. Sci. Eng. Technol. 3(3), 2641–2648 (2014)*